Reg. No. : | | | | | | | | | | |

K 4405

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2009.

Third Semester

Mechatronics Engineering

MH 1201 — DIGITAL ELECTRONICS

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert decimal 65,535 to its hexadecimal and binary equivalents.

2. Draw the NANA-NAND circuit for the equation $Y = AB + AC + AD + BCD$.

3. What do you mean by binary decoder?

4. Show this subtraction in binary form $47_{10} - 23_{10}$.

5. Determine the number of flip-flops needed to construct a shift register capable of storing hexadecimal numbers up to F.

6. Define the term mask-programmable.

7. What are races and cycles?

8. What is a sequential circuit? Give an example.

9. Draw the block diagram of PLA.

10. Give the notations used in an ASM chart.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Assuming 8-bit word length, express the following decimal numbers in sign magnitude, one's complement, and two's complement forms.

(1) – 39 (2) – 120. (8)

(ii) Simplify the following three variable expression using Boolean algebra : $Y = \pi M(3, 5, 7)$. (8)

Or

(b) (i) Implement the following function using NOR-NOR logic. (6)

$Y = AC + BC + AB + D$.

(ii) Using Karnaugh map, simplify the following function : (10)

$f(A, B, C, D) = \overline{A}\,\overline{B}C + AD + B\overline{D} + C\overline{D} + A\overline{C} + \overline{A}\,\overline{B}$.

12. (a) (i) What is an encoder? Draw the logic symbol for decimal to BCD encoder and give its truth table. (10)

(ii) Draw the circuit of 4-bit parallel adder/subtractor and explain its operation. (6)

Or

(b) (i) Design a combinational logic circuit using a PROM. The circuit accepts 3-bit binary number and generates its equivalent excess-3 code. (10)

(ii) State the condition for $B = I_2$ in the Boolean expression (6)

$B = I_0\overline{S}_0\overline{S}_1 + I_1\overline{S}_0S_1 + I_2S_0\overline{S}_1 + I_3S_0S_1$.

What is the combinational logic circuit realized by the above expression?

13. (a) (i) Write short notes on :

(1) Edge triggered flip=flop

(2) Master-Slave flip-flop. (8)

(ii) A synchronous counter with three JK flip-flops has the following connections : (8)

$J_A = K_A = \overline{Q}_C, J_B = K_B = Q_A, J_C = Q_A Q_B, K_C = Q_C$.

Determine its modulus and the count sequence.

Or

(b) (i) Draw the schematic of MOS static RAM cell. How read and write operations are performed in that cell? (8)

(ii) Draw the read and write cycle timing waveforms for the above memory cell and discuss the timing parameters. (8)

14. (a) (i) Discuss the steps involved in the design of asynchronous sequential circuit. (6)

(ii) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is zero, the output does not change for any change in X. Use SR latch for the implementation of the circuit. (10)

Or

(b) (i) Explain static, dynamic, and essential hazards in digital circuit. (8)

(ii) Give hazard-free realization for the following Boolean function: (8)

$f(A, B, C, D) = \sum m\,(0, 2, 6, 7, 8, 10, 12)$

15. (a) Draw an ASM chart and state table for the synchronous circuit having the following description :

"The circuit has a control input X, clock, and outputs A and B. If $X = 1$, on every clock rising edge the code on BA changes from $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$ and repeats. If X = 0, the circuit holds the present state". (16)

Or

(b) Construct state table and design a sequential circuit for ASM chart given below : (16)