G 6016

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

First Semester

Applied Electronics/ VLSI Design

AN 1602 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to ES 1601 – Advanced Digital System Design for M.E. – Embedded System Technologies)

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Mealy model and moore model.

2. What is an ASM chart and give an example?

3. List the steps involved in the design of ASC.

4. What do you mean by state assignment?

5. What are the advantages of compact algorithm.

6. How does the architecture of a PAL differ from that of a PROM?

7. What capability does a polarity fuse give a PLD designer?

8. List two advantages of GAL devices over PAL devices.

9. Write the VHDL code for the Half Adder Circuit.

10. What is a complete sequential system?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Using D-Filpflops design a counter that goes through the following sequence 0, 3, 5, 7, 2, 6 and repeat. (10)

(ii) With an example explain state table assignment and reduction. (6)

Or

(b) (i) Design a BCD counter using state table assignment and reduction method. (10)

(ii) Write short notes on ASM Realization. (6)

12. (a) (i) With example discuss essential and dynamic hazards in asynchronous circuits. (10)

(ii) Explain races in ASC. (6)

Or

(b) Design a sequential combinational lock circuit. The circuit must have a 3-bit combination entry input and an enter button. If the correct sequence of 3-bit values is entered (101 <enter>, 100<enter>, 111<enter>, an output bit will go high, unlocking a door. (16)

13. (a) Explain

(i) Compact algorithm.

(ii) Boolean Difference method. (8 + 8)

Or

(b) (i) Write the PLD description for the 3 to 8 line decoder. (8)

(ii) Explain the Kohavi algorithm. (8)

14. (a) Write out a source file that would program a GAL 16V8A to function as a

(i) 74LS138 (3 to 8) line decoder. (8)

(ii) MOD 8 Binary counter. (8)

Or

(b) Design a digital system that will indicate which contestant in a quiz answers a question first. The system must have a momentary contact push button input for each of six contestants and six LED's to indicate which contestant hit the button first. A reset push button must be provided for the host to clear all lights. (16)

15. (a) Write the VHDL code for serial adder and binary multiplier.

Or

(b) Write the VHDL code for a simple microprocessor.
