G 6017

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

First Semester

Applied Electronics

AN 1603 — VLSI DESIGN TECHNIQUES

(Common to M.E. – VLSI Design)

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the characteristics for enhancement and depletion mode MOS transistors.

2. Define threshold voltage and give its equation.

3. Write the properties of dynamic CMOS logic gates.

4. Draw the stick diagram of a two-input CMOS AND gate.

5. What is sheet resistance? Write its expression.

6. What is meant by stage ratio in inverters?

7. Draw the circuit of a logarithmic shifter.

8. Define stuck-at-1 fault.

9. State two ways to override a parameter value at compile time.

10. What is the difference between a gate instantiation and a module instantiation?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the effect of Body effect. (4)

(ii) Derive the ideal, first order DC equations describing the behaviour of an nMOS device. (12)

Or

(b) Explain the basic steps in n-well CMOS fabrication. (16)

12. (a) (i) Explain the dc characteristics of a CMOS inverter. (10)

(ii) What is noise margin of a CMOS inverter? Explain. (6)

Or

(b) (i) Use a combination of CMOS gates to realise the following functions :

$$Z = A.\overline{B}.\overline{C} + \overline{A}.\overline{B}.C + \overline{A}.\overline{C}.B + A.B.C$$

$$F = \overline{((A + B + C).D)}$$ (6)

(ii) Explain the basic principles of dynamic CMOS design. (10)

13. (a) (i) Draw a diagram to show the parasitic capacitances of a MOS transistor. Give expressions for the various capacitive components. (8)

(ii) Write notes on transistor sizing. (8)

Or

(b) (i) Derive the expression for the total power dissipation in a CMOS circuit. (10)

(ii) Explain why different criteria should be used to size transistors in tightly coupled small-fan-out circuits compared to widely spaced high-fan-out circuits. (6)

14. (a) Explain the design of the following types of adders :

(i) Ripple carry adder.

(ii) Carry look ahead adder.

(iii) High speed adders. (16)

Or

(b) (i) Discuss the issues in Design for Testability. (8)

(ii) Write notes on the clock distribution techniques used in design of circuits. (8)

15. (a) (i) Write notes on the data types used in verilog HDL. (8)

(ii) Given a memory of size 64 words, with 8 bits per word, write verilog code to swap the contents of memory in reverse order, that is, transfer word at 0 to word at 63, word1 to word 62, and so on. (8)

Or

(b) (i) Using the module MUX 4X1, write a structural model for a 16-to-1 multiplexer. (10)

(ii) Write notes on the techniques for writing test benches. (6)