G 6022

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

Elective

Applied Electronics

AN 1625 — ASIC DESIGN

(Common to M.E.–VLSI Design)

(Regulation 2005)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the basic difference between conventional ICS and ASICS?

2. Draw the CMOS logic delay characteristics of an inverter.

3. What is an antifuse? Draw the schematic of an Actal antifuse.

4. Enlist the salient features of reconfigurable gate array.

5. What is meant by crow bar current? Why is it important in output drivers and clock buffers?

6. What are the problems associated with cell library?

7. Why is parallel fault simulation necessary in ASIC design?

8. Distinguish between structures and procedures in VHDL.

9. What are the objectives of detailed routing?

10. What is power routing?

PART B — (5 × 16 = 80 marks)

11. (a) (i) What are the steps involved in VLSI design flow? Explain in detail. (10)

    (ii) Compare semi custom and full custom design in ICS. (6)

    Or

    (b) Briefly explain the influence of paracitic capacitance and propagation delay in CMOS transistor. (16)

12. (a) (i) Explain the two types of antifuses. Mention its advantages and disadvantages. (10)

    (ii) What is PREP? Mention the Benchmark circuits of PREP. (6)

    Or

    (b) What are the different types of I/O requirements in ASIC design? Explain.

13. (a) (i) With a neat sketch explain the two types of gate array ASICS. (8)

    (ii) What are the programming technologies required for Actel and Xilinx FPGAs? Explain. (8)

    Or

    (b) Discuss CAD tools for cell based design and layout. (16)

14. (a) (i) What is the importance of port map command? Using port map command write the VHDL code for full adder using half adder circuit. (10)

    (ii) Write down the importance of (1) If statement (2) Case statement in VHDL. (6)

    Or

    (b) (i) Write a note on FSM synthesis in VHDL. (8)

    (ii) Briefly explain static timing analysis and net capacitance in VHDL. (8)

15. (a) Explain the following in the context of floor planning and placement

    (i)   Cyclic constraints   (6)

    (ii) Channel routing   (5)

    (iii) Clock planning.   (5)

Or

(b) Briefly explain left edge and area routing algorithms.

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