G 6028

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

Second Semester

Applied Electronics

AN 1651 — ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Common to M.E. – VLSI Design)

(Regulation 2005)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the small signal model of MOS transistor and define each parameter.

2. Find the drain current and the transconductance for an NMOS transistor operating with $V_{GS} = 2.5$ V, $V_{tn} = 1$ V, $K_n = 1$ mA/V^2.

3. What is an emitter follower circuit? Give an application for the same.

4. Define $S_{V_{DD}}^{V_{ref}}$ and its significance.

5. What are the various noise signals present in an operational amplifier?

6. Is "Slewing" – a large signal behaviour or small signal behaviour? Justify.

7. How does a basic XOR gate function as phase detector?

8. Calculate the input referred noise for a simple CS stage amplifier shown.
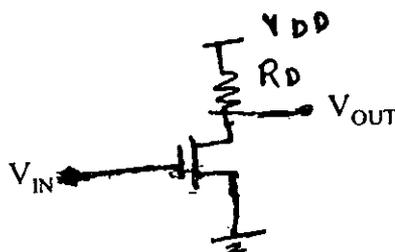
9. Why are active loads advantageous compared to passive loads?

10. Draw the circuit of a simple folded cascode amplifier. State any two of its features.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Analyse the working of MOS in the various regions of operation. (8)

    (ii) Explain the short channel effects in MOS transistors. (8)

Or

(b) (i) Discuss the effect of impact ionization on MOS transistors and draw the MOSFET representation including the effect. (6)

    (ii) Derive the complete small signal model for an NMOS transistor with $I_D = 120$ μA, $V_{SB} = 0.8$ V, $V_{DS} = 2$ V. The device parameters are $\phi_f = 0.3$ V, $W = 12$ μm, $L = 2$ μm, $r = 0.5$ $V^{1/2}$, $k^1 = 200$ μA/V^2, $\lambda = 0.02$ V^{-1}, $t_{ox} = 100$ angstroms, $\psi_0 = 0.6$ V, $C_{sbo} = C_{dbo} = 10$ f F. Overlap capacitance from gate to source and gate to drain is 1 f F. Assume $C_{gb} = 5 f$ F. (10)

12. (a) (i) Draw the circuit of a cascode current source and obtain the expression for V_D min and the output resistance. Compare its performance with folded cascode configuration. (8)

    (ii) Assuming no symmetry for the circuit shown below. Calculate the small signal voltage gain $V_{out}/(V_{in1} - V_{in2})$. (8)
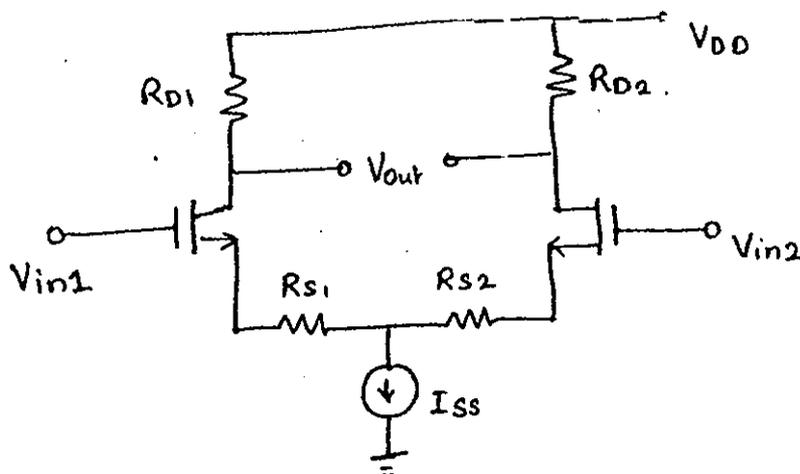
Or

(b) (i) Explain the effect of common mode noise on the differential gain due to mismatch in drain resistance and obtain expression for A_{CM-DM}. (8)

(ii) Draw the circuit of a complementary class AB output stage using common-source output device and its small signal model. Also explain its transfer characteristics. (8)

13. (a) (i) Consider a CMOS Differential pair with current mirror load and discuss its frequency response. (8)

(ii) Explain the effect of noise in operational amplifiers. (8)

Or

(b) (i) Draw the circuit of a telescopic operational amplifier and compare its performance with other types. (10)

(ii) Using the Miller approximation, calculate the –3 dB frequency of a common source transistor stage with following parameters :
$R_S = 1\,k\Omega$, $I_D = 1\,mA$, $k'\dfrac{W}{L} = 100$ mA/V^2, $f_T = 400$ MHz at
$I_D = 1\,mA$, $C_{gd} = 0.5\,pF$, $C_{gb} = 0$, $R_L = 10\,k\Omega$. (6)

14. (a) (i) Explain the following application of PLL

(1) Skew reduction

(2) Frequency synthesis. (5 + 5 = 10)

(ii) Explain the working of two quadrant analog multiplier circuit. (6)

Or

(b) (i) Discuss in detail the different sources of noise in integrated circuits and their characteristics. (10)

(ii) Derive an equation for the lock-range and capture-range in PLL. (6)

15. (a) (i) What are current sink and current source? Draw the circuit of a Widlar current source and explain. (8)

(ii) Explain the working of a class AB amplifier with floating current sources. State its application. (8)

Or

(b) Write notes on MOS telescopic cascode operational amplifier and MOS active cascode operational amplifiers.

G 6028