G 6029

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

Second Semester

Applied Electronics

AN 1652 — COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(Common to M.E. — VLSI Design and M.E. — Computer and Communication)

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the similarities and differences between vector processing and array processing?

2. If the access time to a memory bank is 8 clock cycles, how many memory banks are needed to retrieve one component of a 64 component vector each cycle?

3. Name the three properties to be satisfied by the information stored in memory hierarchy.

4. What are the benefits of memory interleaving?

5. What are the advantages and disadvantages of explicit and implicit parallel programming approaches?

6. What is clock skewing?

7. What is the differences between load balancing and load sharing?

8. Draw the data flow graph for the state merits

   $P = x + y$; $Q = P \div y$; $R = x * P$.

9. Name any two parallel programming languages.

10. Is it possible for the average speed up exhibited by a parallel algorithm to be super linear? Justify.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Give Bell's taxonomy of MIMD computers. (5)

(ii) Draw and explain the architecture of vector super computers. (6)

(iii) Define Amdahl's law for speed up performance. What are its draw backs? How is it overcome in Gustafson's law? (5)

Or

(b) (i) Enumerate the various dependencies to be resolved while exploiting parallelism in detail. (10)

(ii) Draw the dependence graph for the following program segment.

Load R_1, 1000	/ $R_1 \leftarrow 1000$
Load R_2, M(10)	/ $R_2 \leftarrow$ memory (10)
Add R_1, R_2	/ $R_1 \leftarrow R_1 + R_2$
Store M (1000), R_1	/ Memory (1000) $\leftarrow (R_1)$
Store M $((R_2))$, 1000	/ Memory (64) $\leftarrow$ 1000.

where (R_1) means the content of register R_i and memory (10) has 64 initially.

Are there any resource dependencies if only one copy of each functional unit is available in the CPU? (6)

12. (a) (i) Compare the characteristics of CISC and RISC architecture. (5)

(ii) Compare the advantages and draw backs in implementing private virtual memories and a globally shared virtual memory with regard to latency, coherence, page migration, protection, implementation and application problems in a multi computer system. (6)

(iii) Compare the relative merits of four cache memory organizations. (5)

Or

(b) (i) Consider a cache (M_1) and memory (M_2) hierarchy with the following characteristics

M_1 : 16 K Words, 50 ns access time

M_2 : 1 M Words, 400 ns access time

Assume eight word cache blocks, and a set size of 256 words with set associative mapping.

(1) Show the mapping between M_1 and M_2.

(2) Calculate the effective memory access time with a cache hit ratio of $h = 0.80$. (8)

(ii) A 2 – level memory system has 8 virtual pages on a disk to be mapped into four page frames in main memory. Show the successive virtual pages and hit ratio for the following page trace if the LRU, LFU, FIFO page replacement policies are adopted.

1, 0, 2, 2, 1, 7, 6, 7, 0, 1, 2, 0, 3, 0, 4, 5, 1, 5, 2, 4, 5, 6, 7, 2, 4, 2, 7, 3, 3, 2, 3.

Assume that initially the page frames are empty. (8)

13. (a) (i) Enumerate and explain the drawbacks in instruction pipeline design. (6)

(ii) List the solutions that can be used to over come the draw backs. (6)

(iii) Write a note on various message passing mechanisms. (4)

Or

(b) (i) Compare

(1) Static Vs Dynamic pipe line

(2) Linear Vs Non – Linear pipe line

(3) Scalar Vs Vector pipe line. (9)

(ii) Derive the formula for speed up of a K – stage linear pipe line. (4)

(iii) Explain the multi cache coherence problem. (3)

14. (a) (i) Compare the three multi processor hardware organizations. (6)

(ii) Discuss the characteristics of vector processing. (6)

(iii) Discuss about multiple context processors. (4)

Or

(b) (i) Explain the various latency – hiding techniques in multithreaded architectures. (12)

(ii) What are fine grain multi computers? (4)

15. (a) (i) Map nodes of a complete binary tree with four levels to nodes of a 4 – D hyper cube, so that as many tree edges as possible map onto hyper cube edges. (8)

(ii) Explain the various parallel programming models. (8)

Or

(b) (i) What are the draw backs of conventional UNIX for parallel processing? How are they Overcome? (12)

(ii) Write notes on OSF/1 programming environment. (4)
