B 2141

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Third Semester

Computer Science and Engineering

CS 232 — DIGITAL SYSTEMS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How many bits are needed to represent decimal values ranging from 0 to 12,500?

2. State two reasons why some functions have "don't care" terms.

3. Explain why there are $2(2^n)$ functions of n variables.

4. What are the two ways of changing the number of levels in a gate network?

5. Write the logic equation and draw the internal logic diagram for a 4 to 1 MUX?

6. List the different internal digital IC faults.

7. What is meant by the term *edge triggered*?

8. What is the output frequency of a decade counter that is clocked from a 50 KHZ signal?

9. What are the principal differences between synchronous and asynchronous networks?

10. What are hazards?

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following Boolean function by using the tabulation method $F = \sum(0, 1, 2, 8, 10, 11, 14, 15)$. (16)

Or

(b) (i) Simplify the Boolean function $F(w,x,y,z) = \sum(1, 3, 7, 11, 15)$ that has the don't care conditions $d(w,x,y,z) = \sum(0, 2, 5)$. (8)

(ii) State and prove consensus theorem. (8)

12. (a) Design a network of AND and OR gates to convert excess 3 code to 8-4-2-1 BCD code. (16)

Or

(b) (i) Explain the operation of 4 to 10 decoder. (12)

(ii) Realize a multi output network using 4 to 10 decoder. (4)

13. (a) (i) A combinational circuit is defined by the functions $F_1(A,B,C) = \sum(3, 5, 6, 7)$

$F_2(A,B,C) = \sum(0, 2, 4, 7)$ Implement the circuit with a PLA. (8)

(ii) Using ROM, implement a combinational circuit which accepts a 3 bit number and generates an output binary number equal to the square of the input number. (8)

Or

(b) The state table of a sequential circuit is given below :

PS	NS		OUTPUT	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(i) Draw the state diagram, starting from state a, find the output sequence generated with an input sequence 01110010011. (7)

(ii) Reduce the number of states and derive the reduced state table and the reduced state diagram. (5)

(iii) Show that both the circuits are equivalent. (4)

14. (a)

(b)

15. (a)

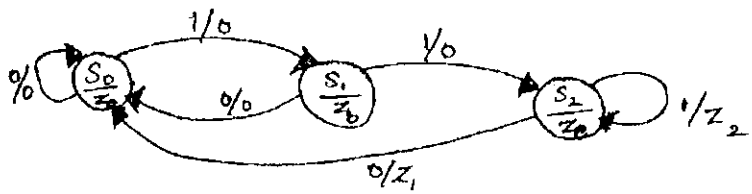
(b)

14. (a) Explain the operation of 4-bit binary ripple counter. (16)

Or

(b) Explain the operation of BCD counter. (16)

15. (a) A state graph for a sequential machine is given below:



Convert it to an SM chart and draw the timing chart with an input sequence 111000. (16)

Or

(b) An asynchronous network has two inputs and one output.

The input sequence $X_1 X_2$ = 00,01,11 causes the output to become 1.

The next input change then causes the output to return to 0.

No other i/p sequence will produce a 1 output.

Construct the state diagram using primitive flow table. (16)