A 1159

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Sixth Semester

Computer Science and Engineering

CS 340 — COMPUTER ARCHITECTURE — II

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define a big endian and small-endian.

2. How the compiler will generate efficient and correct code?

3. What is pipelining? How to measure the speed from pipelining.

4. Define dynamic scheduling with an example.

5. Why hardware-based speculation is important?

6. Compare between scalar and vector processors.

7. Define cache coherence protocol. Mention the classes of CCP.

8. List out the demerits of distributed shared-memory architecture.

9. What are the two major advantages and disadvantages of the bus?

10. Is the RISC processor is necessary? Why.

PART B — (5 × 16 = 80 marks)

11. (a) State the Amdahl's law, define speedup and derive the speedup equation. (16)

Or

(b) Consider the unpipelined processor, assume that it has a 1 ns clock cycle and that it uses 4 cycles for ALU operations and branches and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively. Suppose that due to the clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline? (16)

12. (a) Explain in detail how a RISC instruction set can be implemented in a pipelined fashion with five clock cycle. (16)

Or

(b) (i) Define Hazard. Explain the different types of hazards. (8)

(ii) Determine the total branch penalty for a branch-target buffer assuming the penalty cycles for individual mispredictions make the following assumptions about the prediction accuracy and hit rate:

- Prediction accuracy is 90% (for instruction in the buffer).
- Hit rate in the buffer is 90% (for branches predicted taken).

Assume that 60% of the branches are taken. (8)

13. (a) With neat block diagram explain the typical superscalar RISC processor architecture. (16)

Or

(b) What is VLIW? With help of neat block diagram explain architecture of VLIW processor and its pipeline operations. (16)

14. (a) With neat block diagram explain the centralized shared-memory multiprocessor architecture. (16)

Or

(b) Discus the Performance of symmetric shared-memory multiprocessor and their effects with example. (16)

15. (a) (i) What is a bus transaction, Explain the different types of buses.

(ii) Explain the synchronous and asynchronous buses with example. (8 + 8)

Or

(b) Write a note on following

(i) RISC processor. (8)

(ii) SCSI bus. (8)
