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B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Third Semester

(Regulation 2004)

Computer Science and Engineering

(Common to Information Technology)

CS 1202 — DIGITAL PRINCIPLES AND SYSTEMS DESIGN

(Common to B.E. (Part-Time) Second Semester Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the advantage of gray codes over the binary number sequence?

2. Simplify the following Boolean function :
   (a) $x(x'+y)$
   (b) $xy + x'z+yz$

3. What is a full adder?

4. What are the modeling techniques available to build HDL module?

5. What is a priority encoder?

6. Mention any two applications of multiplexers.

7. How can a D flip flop be converted into a T flip flop?

8. How many states are there in a 3-bit ring counter? What are they?

9. What are the assumptions made for pulse mode circuit?

10. What is a hazard in combinational circuits?

PART B — (5 × 16 = 80 marks)

11. (a) Using Tabulation method simplify the Boolean function

$F(w, x, y, z) = \sum (1, 2, 3, 5, 9, 12, 14, 15)$ which has the don't care conditions $d(4, 8, 11)$

Or

(b) Reduce the Boolean function using K-Map technique and implement using gates $F(w, x, y, z) = \sum (0, 1, 4, 8, 9, 10)$ which has the don't care conditions $d(w, z, y, z) = \sum (2, 11)$.

12. (a) (i) Design a combinational circuit to convert BCD to gray code. (12)

(ii) Design a 4 bit subtractor. (4)

Or

(b) (i) Design a combinational circuit to convert Excess-3 code to BCD code. (10)

(ii) Design a 2 bit × 2 bit multiplier. (6)

13. (a) (i) Implement the Boolean function using 8:1 multiplexer.

$F(A, B, C, D) = A'BD' + ACD + B'CD + A'C'D.$ (8)

(ii) What are advantages of PLA over ROM? Explain the internal construction of PLA. (8)

Or

(b) Construct a full adder circuit and write a HDL program module for the same. (16)

14. (a) (i) Explain the operation of D-Type Edge Triggered Flip-Flop. (8)

(ii) Write HDL code for the following Mealy state diagram. (8)
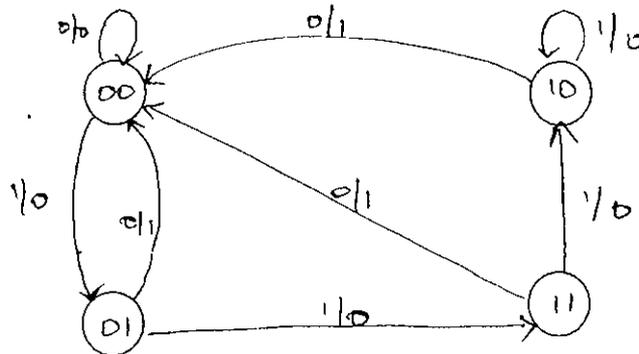
Or

(b) What are the general capabilities of universal shift register? And write the HDL code for the same. (16)

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15. (a) (i) Give hazard-free realization for the following Boolean functions $f(A, B, C, D) = \sum m(1, 3, 6, 7, 13, 15)$. (8)

(ii) Summarize the design procedure for asynchronous sequential circuit. (8)

Or

(b) An asynchronous sequential circuit is described by the following excitation and output function.

$$Y = X_1 X_2 + (X_1 + X_2)Y$$

(i) Draw the logic diagram of the circuit

(ii) Derive the transition table and output map

(iii) Describe the behaviour of the circuit.

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