C 3142

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Fourth Semester

(Regulation 2004)

Computer Science and Engineering

CS 1251 — COMPUTER ARCHITECTURE

(Common to Information Technology)

(Common to B.E. (Part–Time) Third Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Why data bus is bidirectional and address bus is unidirectional in most microprocessors?

2. What are limitations of assembly language?

3. Why floating point number is more difficult to represent and process than integer?

4. Draw a full adder circuit and give the truth table.

5. Define pipeline speedup.

6. State the differences between hardwired and microprogrammed control unit.

7. List the factors that determine the storage device performance.

8. How many 128 x 8 Ram chips are needed to provide a memory capacity of 2048 bytes?

9. Why does DMA have priority over the CPU when both request a memory transfer?

10. What is the advantage of using interrupt initiated data transfer over transfer under program control without interrupt?

PART B — (5 × 16 = 80 marks)

11. (a) (i) What is a stack? Illustrate the use of stack in subroutine processing with suitable diagram. (8)

(ii) Describe different types of addressing modes in detail. (8)

Or

(b) (i) Briefly explain any six I/O operations with an example. (9)

(ii) Illustrate memory read and write operations. (7)

12. (a) (i) Give the block diagram of the hardware implementation of addition and subtraction of signed number and explain the operations with flow chart. (10)

(ii) Explain the representations of floating point numbers in detail. (6)

Or

(b) (i) Design a multiplier that multiplies two 4-bit numbers. (8)

(ii) Describe the algorithm for integer division with suitable example. (8)

13. (a) (i) Explain the execution of an instruction with diagram. (8)

(ii) Explain the function of a six segment pipeline and draw a space diagram for a six segment pipeline showing the time it takes to process eight tasks. (8)

Or

(b) (i) Explain how the performance of the instruction pipeline can be improved. (10)

(ii) Explain multiple bus organization in detail. (6)

14. (a) (i) What is virtual memory? Explain how the logical address is translated into physical address in the virtual memory system with a neat diagram. (10)

(ii) Describe the organization of a typical RAM chip. (6)

Or

(b) (i) Explain the organization of magnetic disk in detail. (6)

(ii) A digital computer has a memory unit of 64 K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the cache accommodate? (10)

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (8)

(ii) Describe the functions of SCSI with a neat diagram. (8)

Or

(b) (i) What is the importance of an I/O interface? Compare features of SCSI and PCI interfaces. (6)

(ii) What are the different input and output signals of DMA controller? Why are the read and write control signals are bidirectional? Under what condition and for what purpose they are used as inputs and outputs? (10)