B 2200

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Fifth Semester

Electrical and Electronics Engineering

EE 333 — DIGITAL SYSTEMS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert 1011101010_2 to octal and hexadecimal numbers.

2. What is the BCD equivalent for the Gray code 1110?

3. Expand the function $F(A, B, C) = A + B'C$ to standard sum of products form.

4. Using K -map find minimum sum of products for the function

$$f(a, b, c) = \Sigma m\ (0, 1, 5, 6, 7).$$

5. Define propagation delay.

6. Implement 2 input NOR gate using CMOS logic.

7. Draw the logic diagram of Master Slave JK flip flop.

8. What are the different of operation in asynchronous sequential circuits?

9. Implement the given function in 4 : 1 multiplexer $F = \Sigma m\ (0, 1, 3, 5, 6)$.

10. Design a 2 bit up counter using PROM.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Convert 0.95 decimal number to its binary equivalent. (6)

(ii) Perform $(756)_8 - (637)_8 + (725)_{16}$. Express the answer in octal form. (10)

Or

(b) (i) Perform the addition in excess-3 code 16 + 29. (6)

(ii) Write short notes on error detection and correction codes. (10)

12. (a) Using K-map simplify the function

$$F = \Sigma m(4, 5, 6, 7, 9, 11, 13, 15, 16, 18, 27, 28, 31)$$

Also find products of sum function. (16)

Or

(b) Find minimum sum of product function using Quine-McClusky method

$$f(a, b, c, d) = \Sigma m\ (1, 3, 4, 6, 11) + \Sigma d\ (0, 8, 10, 12, 13)$$

(16)

13. (a) Design a 4 bit adder/subtractor using logic gates and explain its operation. (16)

Or

(b) (i) Compare TTL and CMOS logic families. (6)

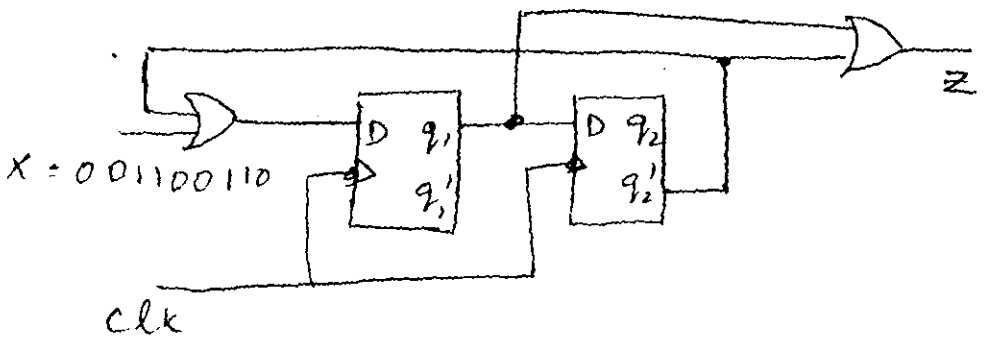
(ii) Draw the block diagram of a BCD adder and explain its operation. (10)

14. (a) (i) Realise D and T flip flops using JK flipflops. (8)

(ii) Write the excitation tables of SR, JK, D and T flipflops. (8)

Or

(b) (i) Find the output sequence 'Z' in Fig. 1



(8)

(ii) Write short notes on memories. (8)

15. (a) Implement the given function using PAL and PLA (16)

$F_1 = \Sigma m(0, 1, 2, 4, 6, 7)$

$F_2 = \Sigma m(1, 3, 5, 7)$

$F_3 = \Sigma m(0, 2, 3, 6)$

Or

(b) Design a synchronous counter that counts in the sequence 0, 1, 3, 5, 7, 4, 2, 0, 6 ... using D flip flops. (16)