A 1224

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Sixth Semester

Electrical and Electronics Engineering

EE 350 — COMPUTER ARCHITECTURE

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the phases of an instruction cycle?
2. What is a stack? How the elements of a stack are accessed?
3. Write the steps needed for performing two's complement arithmetic.
4. What is the special feature of bit sliced processor?
5. What is a PLA? What is the role played by PLA in control unit?
6. What is a nanomemory?
7. Compare Auxiliary memory and Cache memory in terms of usage.
8. What is the difference between page and block?
9. What is the purpose of the communication link between central computer and peripheral device?
10. What is programmed I/O?

PART B — (5 × 16 = 80 marks)

11. (a) (i) What are the different types of basic instruction formats? Explain each type with examples. (8)

(ii) What is the difference between register addressing and direct addressing? Is it possible to combine register addressing and directing addressing? Explain. (8)

Or

(b) (i) Write a program to compute the following expression using Zero address instruction.

$X = (A + B)/(C - D + E)$ (8)

(ii) List the basic registers and explain how the data are transferred to the registers. (8)

12. (a) (i) Draw the flow for performing two's complement multiplication using Booth's algorithm and explain. (10)

(ii) Explain the working of a BCD adder. (6)

Or

(b) (i) Explain the Hardware divide algorithm and explain why it is referred as restoring algorithm. (8)

(ii) Write the steps needed for performing floating point arithmetic operations. (8)

13. (a) (i) What are the address sequencing capabilities required in a control memory? Explain. (8)

(ii) What are the components of hardwired control unit? Explain its working. (8)

Or

(b) (i) Draw the diagram of microprogrammed control unit and explain the functions of each unit. (8)

(ii) Write notes on microinstruction formats. (8)

14. (a) (i) Explain how a virtual memory is implemented using Demand paging. (10)

(ii) Explain memory interleaving and Locality of reference. (6)

Or

(b) (i) Discuss the various design issues of Cache memory. (10)

(ii) Explain how read and write operations are performed in Associative memory. (6)

15. (a) What is an IOP? Explain how communication takes place between CPU and IOP. (16)

Or

(b) Explain the various modes of data transfer. (16)
