# B 2267

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2007.

Third Semester

Information Technology

IF 242 — DIGITAL SYSTEMS DESIGN

Time : Three hours Maximum : 100 marks

Answer ALL questions.

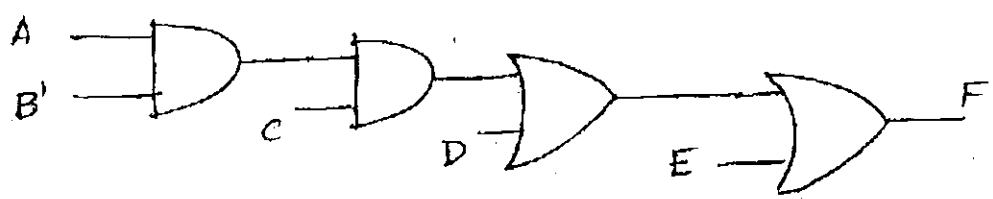
PART A — (10 × 2 = 20 marks)

1. Convert $(AF3.15)_{16}$ to base 10.

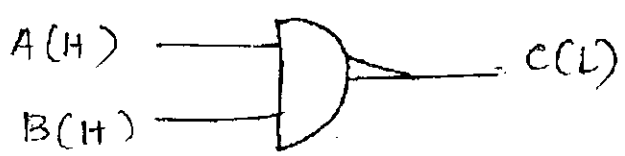
2. Plot the following function by using a K-map and determine its minterm and maxterm lists :

   $f = AB + B\overline{C}$ .

3. Convert the following AND-OR network into an network of NAND gates.




4. Draw the truth table for the following mixed logic gate.

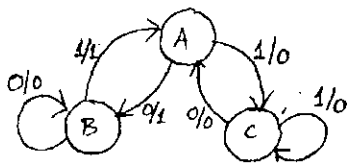



5. Design an Half – Adder circuit.

6. Distinguish between PLA and PAL.

7. Convert T-Flip flop into D-Flip Flop.

8. Determine the output response of the sequential circuit defined in the following figure to the input sequence $x$=011010. (Assume initial state as A).




9. Define static 0 and static 1 hazards.

10. Distinguish between pulse – mode and fundamental-mode asynchronous circuits.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Convert $(18.6)_9$ to $(?)_{11}$ and $(AF.16C)_{16}$ to $(?)_8$. (8)

(ii) Simplify the function
$f(A,B,C,D)=\sum_M(0,5,7,8,10,12,14,15)$ using K-map. (8)

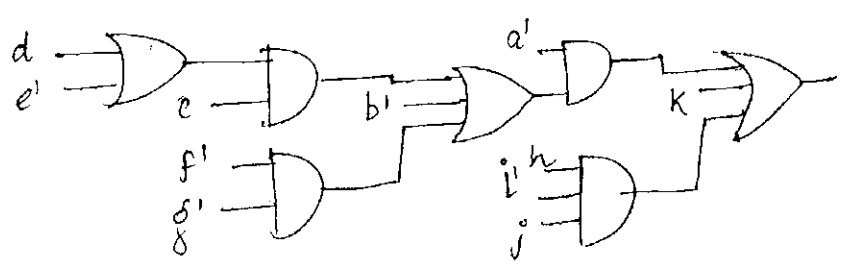
Or

(b) (i) Determine the relationship between the maxterms for the following function and its complement.
$f(A,B,C)=(A+B+\overline{C})(A+\overline{B}+\overline{C})(\overline{A}+B+\overline{C})(\overline{A}+\overline{B}+\overline{C})$ (8)

(ii) Minimize the function using Quine – Mc Cluskey approach.
$f(A,B,C,D,E)=M(2,3,7,10,12,15,27)+d(5,18,19,21,23)$ (8)

12. (a) (i) Write the procedure for designing a minimum two-level NAND-NAND network and minimum two-level NOR-NOR network. (8)

(ii) Convert the following AND-OR network for $F_1$ to the corresponding NAND network. (8)




AND-OR network

Or

(b) Find a network of AND and OR gates to realize.

$f(a,b,c,d)=\sum m(1,5,6,10,13,14)$. Consider solutions with two levels of gates and three levels of gates. Try to minimize the number of gates and the total number gate inputs. Assume that all variables and their complements are available as inputs. (16)

13. (a) Design a binary to Gray code converter using a four-input, four output PROM. (16)

Or

(b) (i) Realize the following three switching functions with a three-input, three-output PROM.

$f_1(A,B,C)=AB+\overline{B}C$

$f_2(A,B,C)=(A+\overline{B}+C)(\overline{A}+B)$

$f_3(A,B,C)=A+BC$ (8)

(ii) Give the PAL realization for the following three expressions. (8)

$f_\alpha(A,B,C,D)=\overline{A}\,\overline{B}\,\overline{D}+\overline{B}C\overline{D}+\overline{A}BCD$

$F_\beta(A,B,C,D)=\overline{A}B+\overline{B}C\overline{D}$

$f_\gamma(A,B,C,D)=\overline{A}B\overline{C}+\overline{B}C\overline{D}+\overline{A}BCD$ .

14. (a) Design a BCD to Excess – 3 code converter using JK flip flops and logic gates. (16)

Or

(b) Find all the equivalent states in the following state table using the implication table method.

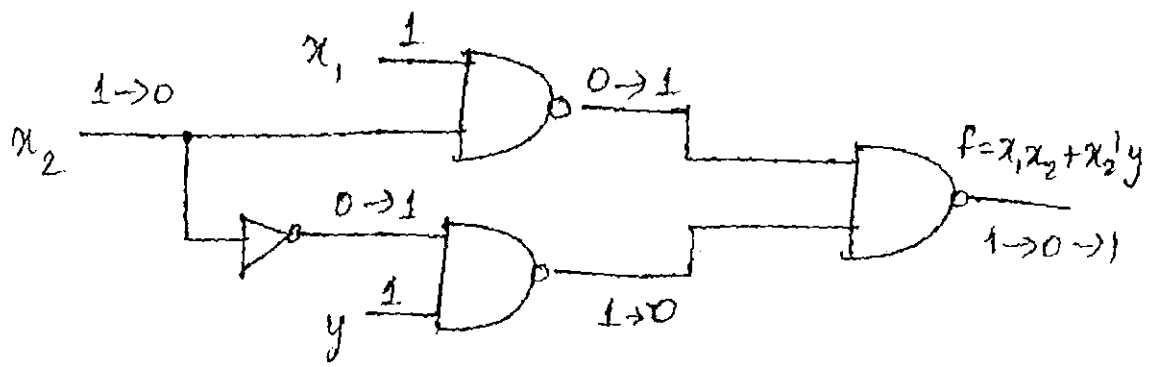
| Present state | Next state | | Present output |
|---|---|---|---|
| | $X=0$ | 1 | |
| a | d | c | 0 |
| b | f | h | 0 |
| c | e | d | 1 |
| d | a | e | 0 |
| e | c | a | 1 |
| f | f | b | 1 |
| g | b | h | 0 |
| h | c | g | 1 |

(16)

15. (a) Design a synchronous sequential circuit using T-Flip Flop with one input line and one output line that recognizes the input string $x=1111$. The circuit is also required to recognize overlapping sequences. (16)

Or

(b) (i) Design a Hazard free network for the following Hazardous Network. (8)




(ii) Design a hazard free circuit for $f=\Sigma(1,3,4,5)$ (8)