

G 6557

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

Elective

Applied Electronics/VLSI Design

VL 1622 — LOW POWER VLSI DESIGN

(Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the five levels of Hierarchy of limits of power dissipation.
2. What is the basic principle of low power design?
3. What is a gate delay model?
4. List few circuit techniques for reducing power consumption.
5. What is CMOS Floating Node?
6. What is a low swing bus system?
7. What are the various power estimation techniques?
8. What is a Signal Entropy Analysis?
9. How a behavioral level can produce a large improvement in power dissipation?
10. List the various sources of software power dissipation.

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail the Physics of power dissipation in submicron MOSFET.

Or

- (b) Discuss in detail any four limits of Low Power design.

12. (a) Explain in detail the circuit level low power design.

Or

- (b) Explain the various circuit techniques for reducing power consumption in Multipliers.

13. (a) Explain the techniques of reducing power consumption in Memories.

Or

- (b) Explain the special techniques for the power reduction in Clock networks.

14. (a) Explain in detail the logic level power estimation techniques.

Or

- (b) Explain Gate level logic simulation and Architecture level Analysis.

15. (a) Explain the behavioral level transforms in detail for improving power dissipation

Or

- (b) Explain in detail the software power optimization method.
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