G 6565

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

Second Semester

VLSI Design

VL 1651 — COMPUTER AIDED DESIGN OF VLSI CIRCUITS

(Common to M.E. - Applied Electronics)

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare semi custom and full custom design methodologies.

2. Define a directed graph and give a data structure to represent it.

3. What is the need for design rules?

4. List the applications of circuit partitioning in VLSI design process.

5. What is shape function? Give an example.

6. Distinguish between local and global routing.

7. Compute the prime implications of the function $F = abc + abc' + acb'$ and represent it on the three dimensional Boolean cube.

8. List the advantages of event driven simulation as compared to compiler driven simulation.

9. Represent the following operations as a data flow diagram

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while (a < b)
    a = a% b
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10. What is the use of retiming in high level synthesis?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Discuss the various semi custom VLSI design methodologies and compare them. (8)

(ii) Explain an algorithm to find the minimum spanning tree with suitable example. (8)

Or

(b) (i) Explain the various steps involved in the VLSI design process, clearly indicating the various CAD tools used. (10)

(ii) With a flowchart explain the depth first search graph algorithm. (6)

12. (a) (i) Explain the constructive placement algorithm with suitable example. How does it differ from iterative placement algorithm? (10)

(ii) What is layout compaction? Explain. (6)

Or

(b) Explain the Kernighan-lin partitioning algorithm with suitable example. (16)

13. (a) (i) List and explain the various graph forms by which a floor plan can be represented. (8)

(ii) Draw the schematic diagram of a JK flip flop using NAND gates and represent it as (1) tripartite graph (2) bipartite graph. (8)

Or

(b) Illustrate the various phases of the Lee algorithm for routing. What are its limitations for large circuits? (16)

14. (a) Draw the diagram of a nMOS 2 input NAND gate and assign suitable strength values. Illustrate the switch level simulation algorithm when applied to the above circuit. (16)

Or

(b) (i) Define tautology. Determine whether the function $f = ab'c' + a'b + bc'$ is a tautology. (6)

(ii) Discuss the various steps involved in two level logic synthesis. (10)

15. (a) Describe the ASAP scheduling algorithm. Explain its role in high level synthesis. (16)

Or

(b) (i) Explain the various steps involved in high level synthesis. (8)

(ii) What is data flow diagram? Explain the various units of DFD with suitable examples. (8)
