G 6230

M.E. DEGREE EXAMINATION, MAY/JUNE 2007.

Embedded System Technologies/Power Electronics and Drives

Elective

ES 1671 — VHDL

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the difference between a signal and a variable.

2. Define test bench.

3. What is a record?

4. Define elaboration.

5. List the difference between function and procedure.

6. Define overloading.

7. Write the syntax for generic command in VHDL.

8. What is the difference between entity and component declaration?

9. Identify the error in the following VHDL fragment :

```
Type real_ptr is access real;
Variable r: real_ptr;
.....
r:= new real;
r := r + 1 .0;
```

10. Define fork module.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Briefly outline the purposes of the following VHDL modeling constructs : entity declaration, behavioral architecture body, structural architecture body, process statement, signal assignment and port map. (8)

(ii) Write a model that represents a simple ALU with integer inputs and output, and a function select input of type bit. If the function select is '0', the ALU output should be the sum of the inputs; otherwise the output should be the difference of the inputs. (8)

Or

(b) (i) Write an entity declaration and a behavioral architecture body for a two input multiplexer, with input ports a, b and sel and an output port z. If the sel input is '0', the value of a should be copied to z, otherwise the value of b should be copied to z. Write a test bench for the multiplexer model and test it using a VHDL simulator. (8)

(ii) Write a model for a counter with an output port of type natural, initially set to 15. When the clk input changes to '1', the counter decrements by one. After counting down to zero, the counter wraps back to 15 on the next clock edge. (8)

12. (a) (i) Develop a model for a priority encoder with a 16 — element bit vector input port, an output port of type natural that encodes the index of the leftmost '1' value in the input and an output of type bit that indicates whether any input elements are '1'. (8)

(ii) Trace the transactions scheduled on the driver for x by the following statements, and show the values taken on by x during simulation. Assume x initially has the value zero.

X <= reject 5ns inertial 1 after 7 ns, 23 after 9 ns, 5 after 10 ns, 23 after 12ns, –5 after 15ns;

Wait for 6ns;

X<= reject 5 ns inertial 23 after 7 ns; (8)

Or

(b) (i) Develop a model of a 3 to 8 decoder and a test bench to exercise the decoder. In the test bench, declare the record type and a constant array of test record values. Initialize the array to a set of test vectors for the decoder, and use the vectors to perform the test. (8)

(ii) Device a sequence of input values for the Multiplier Accumulator (MAC) that cause the sum in the accumulator to overflow. (8)

13. (a) (i) Write parameter specifications for the following signal-class parameters.:

- a bit signal, clk, to be assigned to by a procedure, and
- an unconstrained standard-logic vector signal, data_in, whose value is to be read by a procedure. (8)

(ii) Write an alias declaration that defines the name cons as an alias for the predefined operation "&" with a character left argument, a string right argument and a string result. (8)

Or

(b) (i) Write a function, returning a Boolean result, that tests whether a standard logic signal currently has a valid edge. A Valid edge is defined to be a transition from '0' or 'L' to '1' or 'H' or vice versa. Other transitions, such as 'X' to '1', are not valid. (8)

(ii) Write a declaration for a procedure that increments an integer, as the procedure declaration would appear in a package declaration Also write a declaration for a function that tests whether an integer is odd, as the function declaration would appear in a package declaration. (8)

14. (a) (i) Develop a behavioral model of a tristate buffer with data input, data output and enable ports, all of type std_logic. The propagation time from data input to data output when the buffer is enabled is 4 ns. The turn on delay from the enable port is 3 ns, and the turn-off delay is 3.5 ns. (8)

(ii) Develop a package of component declaration for two input gates and an inverter, corresponding to the logical operators in VHDL. Each component has ports of type bit and generic constants for rising output and falling output propagation delays. (8)

Or

(b) (i) Develop a behavioral model of a multiplexer with n select inputs, 2^n data inputs and one data output. (8)

(ii) Develop a structural model for an n bit-wide ripple-carry adder. The least significant bits are added using a half adder component, and the remaining bits are added using full-adder components. (8)

15. (a) (i) Write a type declaration for an access type that points to a string object. Declare a variable of the type, initialized by allocating a string of four spaces. Write a statement that changes the first character in the string to the character NUL. (8)

(ii) Suppose that the next line in a text file contains the characters.

123 4.5 6789

What is the result returned by the following read calls?

readline(in_file,L);

read(L, bit_value);

read (L ,int_value);

read (L, real value);

read(L,str_value);] (8)

Or

(b) (i) Develop an Abstract Data types (ADT) for last-in/first-out stacks of objects. The ADT should be parameterized by the type of object and should provide operations to create a new stack, to test whether a stack is empty, to push an object onto the stack and to pop the top object from the stack and return the object's value. (8)

(ii) Write declarations and statements to create and initialize a random number generator using the random package. The numbers should be uniformly distributed between 1.0 and 2.0. Write a statement that uses the generator to generate a random number in the real variable X. (8)