

G 3501

M.C.A. DEGREE EXAMINATION, MAY/JUNE 2007.

First Semester

MC 1601 — COMPUTER ORGANIZATION

(Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify the Boolean expression, if possible $A + AB + ABC$.

2. Convert the following decimal numbers to binary and add using the 2's complement form: -110 and -84.

How can a decoder be used as a multiplexer?

When is the following register transfer statement possible?

 $T : R2 \leftarrow R1, R1 \leftarrow R2;$

List the micro-operations for fetch and decode phase of basic computer.

An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes a1.

What must be the last two instructions of the output program?

What is the difference between isolated I/O and memory-mapped I/O?

What is the basic advantage of using interrupt initiated data transfer over transfer under program controlled with out an interrupt?

How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

What is locality of reference?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Use Karnaugh map to minimize the following SOP expression :

$$\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + \overline{A}BCD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + \overline{A}BCD + \overline{A}B\overline{C}\overline{D} + \overline{A}BC\overline{D} \quad (8)$$

- (ii) Draw the circuit for full adder from the truth table using K-map. (8)

Or

- (b) Design a 2-bit count-down counter. (16)

12. (a) (i) Construct a 16 to 1 line multiplexer with 2 8 to 1 line multiplexers and explain its operation by means of a function table. (10)

- (ii) Show the block diagram of the hardware that implements the following register transfer statement $P : R2 \leftarrow R1$ (6)

Or

- (b) (i) Given a 64×8 ROM chip with the enable input, show the external connections necessary to construct a 256×8 ROM with four chips and a decoder. (10)

- (ii) Draw the block diagram of 4-bit synchronous binary counter and explain its operation. (6)

13. (a) (i) A computer uses a memory unit with 256 k words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

(1) How many bits are there in the operation code, register code part and the address part?

(2) Draw the instruction word format and indicate the number of bits in each part?

(3) How many bits are there in the data and address inputs of memory? (3 × 2 = 6)

- (ii) Write an assembly program to multiply two positive numbers by repeated addition method. (10)

Or

- (b) (i) How are interrupts handled by the basic computer? Explain the interrupt cycle with a flow chart. (10)

- (ii) Write a sub routine to complement each word in a block of data. The subroutine takes two parameters: the starting address and the number of words in each block. (6)

14. (a) (i) What are interface units? Why are they needed? (6)

- (ii) Explain the Daisy chain method of establishing priority. (10)

Or

- (b) Explain the operation of serial communication processor with necessary protocols. (16)

15. (a) (i) Explain the mapping procedure for converting virtual address to physical address with necessary tables. (10)

- (ii) What is page fault? How is it handled? (3 + 3)

Or

- (b) (i) Explain the various instruction types based on the length. (6)

- (ii) Write a note on the various addressing modes. (10)