Reg. No. : | | | | | | | | | | | |

Q 2200

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Third Semester

Mechatronics Engineering

EC 154 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Using excess-3 code addition procedure, find the sum of the decimal numbers 3 and 5.

2. For each element x in a Boolean algebra prove that $x + 1 = 1$, using Boolean postulates.

3. Define a combinational circuit. Give an example.

4. Differentiate between PAL and PLA.

5. Draw a T flip-flop circuit using JK flip-flop.

6. Give one application each for a serial to parallel and a parallel to serial shift registers.

7. Define an asynchronous sequential circuit.

8. What is the significance of state diagram of a circuit?

9. What is the purpose ASM chart?

10. What are the elements of ASM chart?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Prove the following Boolean identities :

(1) $x + xyz + x'yz + wx + w'x + x'y = x + y$ (3)

(2) $(x_1 + x_2)(x_1' x_3' + x_3)(x_2' + x_1 x_3)' = x_1' x_2$. (4)

(ii) Add $(321)_5$ and $(314)_5$. (2)

(iii) Multiply $(142)_5$ by $(32)_5$. (3)

(iv) Using 2's complement subtract 10010 from 11011. (4)

Or

(b) Minimize the following switching functions using K-map :

(i) $f_1 = \sum m(0, 1, 3, 5, 7, 9, 10) + \sum d(4, 12)$

(ii) $f_2 = \pi m(4, 5, 6, 8, 9, 12, 14) + \sum d(15)$.

Implement the first functions using only NAND gates and the second function using NOR gates. (8 + 8)

12. (a) Design and implement a full subtractor circuit and a 8 to 1 multiplexer circuit.

Or

(b) (i) A combinational circuit is defined by the functions $f_1 = \sum(3, 5, 6, 7)$ and $f_2 = \sum(0, 2, 4, 7)$ implement the circuit with a PLA. (10)

(ii) Given a 32 × 8 ROM chip with an enable input, show the external connections necessary to construct a 128 × 8 ROM. (6)

13. (a) (i) Explain the working of a master-slave JK flip-flop state its advantage. (10)

(ii) Draw a RAM cell and explain its working. (6)

Or

(b) Design and explain the working of a mod-7 up-down counter.

14. (a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and one output z initially both inputs and output are equal to 0 when x_1 or x_2 becomes 1, z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.

Or

(b) (i) Find the circuit that has no static hazards and implements the Boolean function.

$F = \sum(0, 2, 6, 7, 8, 10, 12)$. (8)

(ii) Write notes on races and essential hazards. (8)

15. (a) (i) Construct an ASM chart for a digital system that counts the number of people in a room. People enter the room from one door with a photocell that changes a signal x from 1 to 0 when the light is interrupted. They leave the room with a second door with a similar photocell with a signal y. Both x and y are synchronized with the clock but they may stay on or off for more than one clock period. The data-processor subsystem consists of an up-down counter with a display of its contents. (12)

(ii) Draw the portion of ASM chart that specifies a conditional operation to increment register R during state T_1 and transfer to state T_2 if control inputs Z and y are equal to 1 and 0 respectively. (4)

Or

(b) A digital system consists of two registers R_1 and R_2 and a flip-flop E. The system counts the number of 1's in the number loaded into register R_1 and sets Register R_2 to that number. This is done by shifting each bit from Register R_1 one at a time into flip-flop E. The value in E is checked by the control and each time it is equal to 1, the register R_2 is incremented by 1. The control subsystem uses one external input S to start the operation and two status inputs E and Z from the data processor. E is the output of the flip-flop Z is the output of a circuit that checks the contents of register R_1 for all 0's. The circuit produces an output $Z = 1$ when R_1 is equal to 0. Draw the ASM chart and design the circuits using multiplexers.
