Reg. No. : | | | | | | | | | | |

R 3282

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Third Semester

(Regulation 2004)

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Common to B.E. Part Time Second Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert $(0.513)_{10}$ to octal.

2. Express F = A + B'C as sum of minterms.

3. Draw the logic diagram for X = AB + B'C.

4. Implement F = (AB' + A'B) (C + D') with only NOR gates.

5. What is a Moore machine?

6. Give the characteristic expression of a JK Flip Flop.

7. What is a flow table?

8. What is Race?

9. Draw the logic diagram of a memory cell.

10. What is a combinational PLD?

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Convert the binary number 0.1100 to its equivalent decimal number. (4)

(ii) Convert the number 326_8 to its equivalent decimal number. (4)

(iii) Convert the following binary number to its hexadecimal equivalent 1111110000. (4)

(iv) Convert 2497.50_{10} to its octal equivalent. (4)

Or

(b) (i) Simplify the following using Kmap.

X = A'B + A'B'C + ABC' + AB'C' (4)

(ii) Convert SOP to equivalent POS.

A'B'C + A'B'C + A'BC + AB'C + ABC. (4)

(iii) Apply Demorgan's theorem to the following expression.

((A + B + C) D)' (4)

(iv) Using Boolean Laws and rules simplify the logic expression.

Z = (A' + B) (A + B). (4)

12. (a) (i) Implement Full adder using two half adders. (8)

(ii) Draw and explain the BCD adder circuit. (8)

Or

(b) (i) Implement the Boolean expression using gates

X = (AB + C)' D + E. (4)

(ii) Draw the logic symbol of a XNOR gate and give its truth table. (4)

(iii) Sketh a NAND-NAND logic circuit for the Boolean expression. Y = AB' + AC + BD. (8)

13. (a) Design a 3 bit binary counter using T flip flop that has a repeated sequence of six states. 000 - 001 – 010 – 100 – 101 – 110. Give the state table, state diagram and logic diagram. (16)

Or

(b) Design the sequential circuit whose state table is given as (16)

Present state		Input	Next state		Output
A_1	A_2	x	A_1	A_2	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

14. (a) What are Hazards? Explain in detail with a suitable example. (16)

Or

(b) The circuit has two inputs T (toggle) and C (Clock) and one output Q. The output state is complemented if T = 1 and clock c changes from 1 to 0 (negative edge triggering) otherwise, under any other input condition, the output Q remains unchanged. Derive the Primitive flow table and Implication table. (16)

15. (a) Write short notes on :

(i) RAM. (8)

(ii) Types of ROM's. (8)

Or

(b) Implement the following two Boolean functions with a PLA.

$F_1 (A, B, C) = \sum (0, 1, 2, 4)$

$F_2 (A, B, C) = \sum (0, 5, 6, 7)$ (16)