Reg. No. : | | | | | | | | | | | |

R 3323

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Seventh Semester

(Regulation 2004)

Electronics and Communication Engineering

EC 1401 — VLSI DESIGN

(Common to B.E. (Part-Time) Sixth Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the advantages of SOI CMOS process?

2. Distinguish electrically alterable and non-electrically alterable ROM.

3. Compare nMOS and pMOS devices.

4. Compare enhancement and depletion mode devices.

5. What is meant by continuous assignment statement in Verilog HDL?

6. What is a task in Verilog?

7. Give the application of PLA.

8. What is meant by a transmission gate?

9. What is the aim of adhoc test techniques?

10. Distinguish functionality test and manufacturing test.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw and explain the n-well process. (10)

(ii) Explain the twin tub process with a neat diagram. (6)

Or

(b) (i) Discuss the origin of latch up problems in CMOS circuits with necessary diagrams. Explain the remedial measures. (10)

(ii) Draw and explain briefly the n-well CMOS design rules. (6)

12. (a) (i) Derive expressions for the drain-to-source current in the nonsaturated and saturated regions of operation of an nMOS transistor. (10)

(ii) Define and derive the transconductance of nMOS transistor. (6)

Or

(b) (i) Discuss the small signal model of an MOS transistor. (8)

(ii) Explain the CMOS inverter DC characteristics. (8)

13. (a) (i) Give a Verilog structural gate level description of a bit comparator. (10)

(ii) Give a brief account of timing control and delay in verilog. (6)

Or

(b) (i) Give a Verilog structural gate level description of a ripple carry adder. (10)

(ii) Write a brief note on the conditional statements available in verilog. (6)

14. (a) (i) Compare the different types of ASICs. (10)

(ii) Discuss the operation of a CMOS latch. (6)

Or

(b) Explain the ASIC design flow with a neat diagram. Enumerate clearly the different steps involved. (16)

15. (a) Explain the chip level test techniques. (16)

Or

(b) Explain the system level test techniques. (16)