Reg. No. : | | | | | | | | | | |

Q 2319

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Third Semester

Information Technology

IF 242 — DIGITAL SYSTEMS DESIGN

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write down the octal and binary equivalent of the decimal number 10.725.

2. State De-Morgan's theorem.

3. What is mean by fan-in and fan-out?

4. Implement the Half-Adder circuit using only NAND gates.

5. Distinguish between a decoder and a demultiplexer.

6. Distinguish between a PLA and a PAL.

7. Differentiate between edge and level triggered of flip flops.

8. Why is a synchronous counter faster than a ripple counter?

9. Differentiate between Moore Machine and Mealy Machine?

10. What is fundamental mode and pulse mode sequential circuits?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Use Boolean theorems and prove the following :

(1) $A + BA = A$

(2) $A + \overline{A}B = A + B$

(3) $AB + BC + \overline{B}C = AB + C$

(4) $(A + B)(A + C) = A + BC$. (8)

(ii) Use Boolean theorems and simplify the following :

(1) $ABC + A\overline{B}C + \overline{A}BC + A\overline{B}\,\overline{C} + AB\overline{C} + \overline{A}B\overline{C}$

(2) $(A+B+C)(A+B+\overline{C})(A+\overline{B}+\overline{C})(A+\overline{B}+C)$. (8)

Or

(b) Simplify the following expression

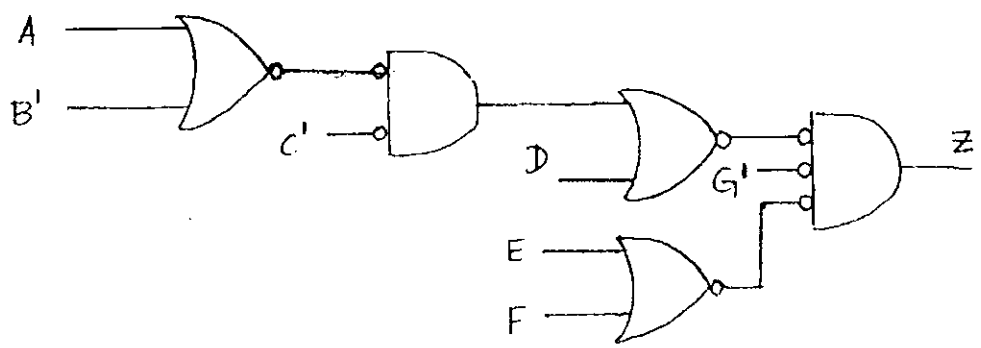
$y = m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{14}$ using

(i) Karnaugh Map (8)

(ii) Quine McCluskey method. (8)

12. (a) (i) Write the procedure used to convert a AND-OR network to a NAND network. (8)

(ii) Draw the equivalent AND-OR network. (8)



Or

(b) Design the mixed-logic hardware to examine two 2-bit binary numbers (A_2A_1 and B_2B_1) and produce a TRUE output if the number B_2B_1 is greater than or equal to the number A_2A_1. The variables A_1 and A_2 are both LT, while B_2, B_1 and the output are HT. (Implement in NAND hardware) (16)

13. (a) (i) Implement the following function with a suitable multiplexer :

$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (8)

(ii) Realize the following functions using suitable PAL device :

$f_1(x, y, z) = \Sigma m(1, 2, 4, 5, 7)$

$f_2(x, y, z) = \Sigma m(0, 1, 3, 5, 7)$. (8)

Or

(b) (i) Implement a full-adder with a suitable decoder. (8)

(ii) Realize a full-adder using suitable PLA device. (8)

14. (a) Design a shift register with parallel load that operates according to the following function table. (16)

Shift	Load	Register Operation
0	0	No change
0	1	Load parallel data
1	x	Shift right

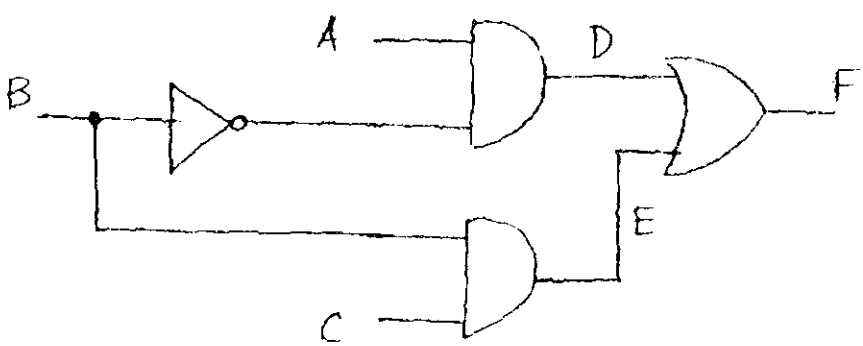
Or

(b) Design a 4-bit binary ripple counter using toggle flip-flops. (16)

15. (a) Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected. (16)

Or

(b) What is a static-0 and static-1 hazard? Illustrate the hazard present in the following network.



Also design a hazard–free network. (16)