Register Number.....

M.E. DEGREE EXAMINATIONS, OCTOBER / NOVEMBER - 2008

Second Semester

APPLIED ELECTRONICS

P07AE201-Analysis and Design of Analog Integrated Circuits

Time: Three Hours **Maximum Marks: 100**

PART A (20 X 1 = 20 Marks)

1. If I = 1mA and β = 100 and V_A = 10V, the transconductance of BJT is _____ mA / V
   A) 10 B) 38.5 C)0.01 D) 0.1

2. In _____ region of operation, the MOS transistor is modeled to have an exponential relationship between control voltage and drain current.
   A) active B) triode C) sub threshold D) cut off

3. The built in voltage of an open circuited pn junction is given by _____
   A) $\varphi_o = V_T \ln (n_i^2 / N_A N_D)$ B) $\varphi_o = V_T \ln (N_A N_D / n_i^2)$
   C) $\varphi_o = 1 / V_T \ln (N_A N_D / n_i^2)$ D) $\varphi_o = 1/ V_T \ln (n_i^2 / N_A N_D)$

4. The effect that exists when source and substrate are at different potential is called
   A) subthreshold conduction B) velocity modulation
   C) Body effect D) short channel effect

5. For a MOS current mirror having identical devices operated in active region, with infinite output impedance, the ratio is _____
   A) infinity B) zero C) 1 D) $(W/L)_1 / (W/L)_2$

6. Using _____ technique the power supply sensitivity can be greatly reduced in voltage references.
   A) bootstrap bias B) start up circuit C) Thermal voltage D) bandgap

7. _____ and _____ are the performance specifications of a well designed output stage in an amplifier
   A) minimum input resistance, high signal power
   B) minimum output resistance, high signal power
   C) low power dissipation, low signal power
   D) Low power dissipation, high output resistance

8. Differential pairs with active loads offer _____
   A)high voltage gain B) high voltage swings
   C) low output resistance D) low voltage gain.

9. The limitation of Miller effect in transistors is _____
   A) neglects poles in transfer function B) neglects body effect
   C) discards the zeros of transfer function D) neglects high frequency effects

10. Common Gate stage is _____
   A) wide band amplifier B) high gain amplifier
   C) input stage of multistage amplifier D) low frequency amplifier

11. _____ opamp is rarely used in Unity gain buffer
A) Differential cascode B) Folded cascode
C) OTA D) Active load Op amp

12. In Differential amplifiers the noise contribution of PMOS and NMOS_____ Transconductance
A) decreases in proportion to B) remains constant irrespective of
C) increases in proportion to D) is infinite compared to

13. _____ gate can be used as phase detector in PLL
A) AND B) OR C) NAND D) XOR

14. _____ represents an anlog circuit where the output frequency if a linear function of its control voltage
A) PLL B) Multiplier C) VCO D) Gilbert cell

15. The noise due to crystal defects is called _____
A) Shot noise B) Thermal noise C) Flicker noise D) Popcorn noise

16. If magnitude of V_1 or V_2 is much smaller than V_T, the multiplier cell functions as
A) modulator B) PLL C) Phase detector D) analog multiplier

17. Matching of current mirror transistors in MOS is improved by
A) varying the gate areas B) Increasing the channel length
C) increasing output resistance D) providing low output swing

18. In CMOS Class AB output stage _____ configuration is well suited for ISDN
A) Common Drain B) CS-CC C) CD-CS D) CD-CC

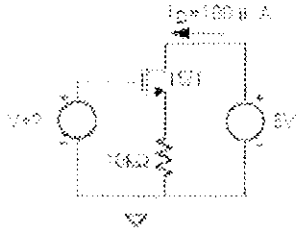
19. _____ amplifiers suffer from the limitation of small output swing
A) Differential B)Telescopic cascade C) Folded cascade D) OTA

20. Compared to cascade amplifiers folded cascade provides _____
A) short channel effect minimization B) increased DC level at output
C) degradation in speed D) large input resistance

PART-B (5 X 16 = 80 Marks)

21a. (i) Draw the MOSFET with all the capacitive effects and name and explain each effect.

(ii) For the circuit shown below, calculate the required gate voltage to achieve a drain current of 100 μA. The effective value of W/L is 15/1. (Assume other parameters)



(OR)

21b. With relevant diagrams explain the operation of MOS in
(i) Triode region

(ii) active region

22a. (i) Explain the Cascode current mirror circuit and obtain expression for output resistance and minimum output voltage.

(ii) Discuss the operation of Band Gap reference circuit

(OR)

22b. Explain the various output stages in analog circuits

23a. (i) For a CS amplifier, derive the expression for transfer function

(ii) Analyse the operation of a Differential amplifier with active load

(OR)

23b. List the various factors that limit the slew rate of opamps and discuss methods for improving the same.

24a. Draw and explain the basic principle of PLL and perform an analysis of first order PLL

(OR)

24b. Discuss the noise model for the integrated circuit components listed:
(i) capacitor , (ii) BJT (iii) OpAmp

25a. What are the various methods of realizing OpAmps. Draw the schematic and explain the realisation

(OR)

25b.(i). For the MOS cascode current sink $g_{m2} = 152.6\mu S$, $g_{ds2} = g_{ds1} = 0.97\mu S$ and $g_{mb2} = 0$. Find the output resistance.

(ii) Compare various current sources with circuits.

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