Register Number.....

M.E. DEGREE EXAMINATIONS: OCTOBER/NOVEMBER - 2008

Second Semester

APPLIED ELECTRONICS

P07AE202: Computer Architecture And Parallel Processing

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions: -

PART A (20 x 1 = 20 Marks)

1. Multiprocessors are called as _____
   A. loosely coupled system B. tightly coupled systems C. symmetric system
   D. None of the above.

2. The time required by a processor to access the memory is called as
   A. Granularity B. Memory latency C. Throughput D. None of the above

3. An n-input Omega network requires _____ stages of 2 x 2 switches.
   A. n^2 B. n logn C. $\log_2 n$ D. None of the above

4. When the number of processors increases, the load on each processor _____
   A. decreases B. increases C. kept constant D. None of the above

5. Both the clock rate and No. of cycles per instruction is less for
   A. Super Pipelined B. Superscalar RISC
   C. VLIW D. Scalar RISC

6. Which property is does not related to Locality of Reference
   A. Temporal B. Spatial
   C. Concurrent D. Sequential

7. Partitioning the main memory into no. of pages with fixed size is
   A. TLB B. Segmentation
   C. Paging D. Address Translation

8. In the cache performance issue, the hit ratio versus cache size can be approximated by
   A. $1+C^{-0.5}$ B. $1+C^{0.5}$
   C. $1-C^{-0.5}$ D. $1-C^{0.5}$

9. Latency sequence is a sequence of permissible _____ between successive task indications
   A. Forbidden latency B. non forbidden latency
   C. latency D. none of the above.

10. Buses implemented on printed circuit boards are called _____
A. data bus B. memory bus C. local bus D. none of the above .

11. Data dependencies among instructions already in the pipeline lead to _____
A. pipeline stalling B. date dependence C. scheduling D. none of the above.

12. . Adaptive routing is mainly used to avoid _____
A. virtual channel B. dead lock C. message routing D.none of the above.

13. f : V→M Corresponds to _____instruction.
A. Vector- Vector B. Vector Store C. Vector load D. gather

14. The Segmentation of long vector into fixed length segment (to match into the length of vector resistor) is defined as_____
A. Vectorization ratio B. Strip-mining C. Balancing D. CVF

15. The efficiency of a single-threaded machine is given by
A. 1/(1+L/R) B. L/R C. 1/(1+R/L) D. None of the above

16. The maximum number of instructions that can be simultaneously executed in the Pipeline is defined as
A. Instruction issue rate B. Instruction issue latency
C. Instruction level parallelism D. simple operation latency

17. _____ is a pure parallel programming language.
A. Fortran B. Linda C. C++ D. Ada

18. An operating system that supports symmetric multiprocessing is _____
A. Unix system V B. Mach / OS kernel C. OSF/1 D. Unix 4.4 BSD

19. The message passing model in which buffers are used in channels is _____ message passing.
A. Synchronous B. Asynchronous C. Shared variable D. Distributed

20. Multitasking at loop control level is defined as
A. Micro tasking B. Macro tasking C. auto tasking D. Mini tasking

PART B (5 x 16 = 80 Marks)

21.a) i) Explain the different models of shared memory multiprocessors. (8)

ii) Explain the various dependencies to be resolved while exploiting parallelism. (8)

(OR)

21. (b) (i) Explain about hardware and software parallelism. (6)

(ii) Explain any two speedup performance laws. (10)

22. (a)Compare the instruction set architecture in RISC and CISC scalar processors and also compare their various characteristics.

(OR)

22. (b) Enumerate the various page replacement policies.

23. (a) i)Enumerate and explain the drawbacks in instruction pipeline design. (8)

ii)List the solutions that can be used to overcome the drawbacks. (8)

(OR)

23. (b) i)Write about the design issues of superscalar and super pipeline (8)

ii) Explain the various message passing mechanisms in parallel architecture (8)

24. (a)Explain the vector instruction types and memory access schemes for the vector Supercomputers

(OR)

24. (b) Explain the principles of multithreading in detail.

25. (a) Explain the various parallel programming models.

(OR)

25. (b) Explain the MACH/OS Kernel architecture.

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