

Register Number.....

M.E. DEGREE EXAMINATIONS: OCTOBER/NOVEMBER 2008

Third Semester

APPLIED ELECTRONICS

P07AEE04 : DSP Integrated Circuits

Time : Three Hours

Maximum Marks:100

Answer ALL Questions:-

PART A (20 x 1 = 20 Marks)

1. Leaf cell is a.....
A. Top Level block B. Bottom Level block C. Standard Cell D. Composition Cell
2. Condition for NMOS transistor to operate in Linear region
A. $V_{gs}-V_t < 0$ B. $V_{gs}-V_t < V_{ds}$ C. $V_{gs}-V_t > V_{ds}$ D. $V_{gs}=V_t$
3. The ECL family has the advantage over CMOS is
A. Low Power B. High Speed C. Simple Circuit D. Good Noise Immunity
4. Which of the following is ratio less logic?
A. NMOS B. PMOS C. CMOS D. BiCMOS
5. Which of the following is not causal?
A. $y[k+1] + 0.64y[k-1] = x[k] + 2x[k-1]$
B. $y[k+1] - 0.64x[k+1] = x[k] + 2x[k-1]$
C. $y[k+1] = x[k] + 2x[k-1]$
D. $y[k+1] + 0.64y[k-2] = x[k] + 2x[k-1]$
6. Which FFT Algorithm is less complex?
A. Cooley & Turkey B. Sande-Turky C. Cook-Toom's D. Winograd's
7. The Delay in DSP blocks are realized using
A. RC Network B. D Flip Flops C. Multiplexers D. Adders
8. What is the basic difference between DFT and FFT
A. DFT has fewer multiplications than FFT
B. DFT is faster than FFT
C. FFT has fewer multiplications than DFT
D. DFT is not suitable for Hardware implementation
9. What is the advantage of Transposed form of FIR Structure
A. Less Complexity B. Less Critical Path delay
C. Less input capacitance D. Low clock speed
10. What is the reason for round off Noise?
A. Truncation of bits in the result B. Signal exceeds available number range
C. Change in sampling rate D. Finite Precision Coefficient representation
11. Zero Input Limit Cycles can be eliminated by
A. Using larger data word length B. Using shorter data word length
C. Increasing the sampling rate D. Decreasing the sampling rate

12. Scaling is not required for
- A. Fixed Point Multiplication
 - B. Floating Point Multiplication
 - C. Signed Multiplication
 - D. Unsigned Multiplication
13. Harvard Architecture is
- A. Common Memory for Program and data
 - B. Separate Memory for Program and data
 - C. Single Address bus
 - D. Single Data Bus
14. Which of the following is Multi Stage interconnection Network?
- A. Cross Bar Architecture
 - B. Square Mesh
 - C. Omega Network
 - D. Single Bus Structure
15. What is the advantage of shared memory Architecture?
- A. Parallel Processing
 - B. Bit Serial Computation
 - C. High Speed Sequential Memory Access
 - D. Perform Complex operation
16. Bit Serial PE
- A. Requires same Clock rate as Parallel PE
 - B. Requires Single wire for data handling
 - C. Requires Multiple wire for data handling
 - D. is a Complex hardware structure
17. A Normalized W_d Binary word in One's Complement representation is
- A. $x = (1 - 2x_0) \sum_{i=1}^{W_d-1} x_i 2^{-i}$
 - B. $x = -x_0(1 - Q) + \sum_{i=1}^{W_d-1} x_i 2^{-i}$ where $Q = 2^{W_d-1}$
 - C. $x = -x_0 + \sum_{i=1}^{W_d-1} x_i 2^{-i}$
 - D. $x = x_0(1 + Q) + \sum_{i=1}^{W_d-1} x_i 2^{-i}$ where $Q = 2^{W_d-1}$
18. Distributed Arithmetic Algorithm is efficient, if it is
- A. Implemented using DSP processor
 - B. Implemented using LUT based FPGA
 - C. Implemented using MUX based FPGA
 - D. Implemented using Microprocessor
19. On-line Arithmetic is a number system with the property
- A. to compute the i^{th} digit of the result from last $(i + k)^{\text{th}}$ digit
 - B. to compute the i^{th} digit of the result from $(i - 1)^{\text{th}}$ digit
 - C. to compute the i^{th} digit of the result from first $(j + k)^{\text{th}}$ digit
 - D. to compute the i^{th} digit of the result from $(i + 1)^{\text{th}}$ digit
20. Residue number system is applicable for
- A. Floating Point Operation only
 - B. Fixed point operation only
 - C. Fixed and Floating point operations
 - D. Logarithmic Number only

PART B (5 x 16 =80 Marks)

21. (a) (i) Draw the circuit of single bit RAM cell with MOS structure and explain the working principle. (8)

(ii) Explain the various fabrication processes of CMOS devices. (8)

(OR)

21 (b) (i)) What are the features of ASIC DSP processors (8)

(ii) List out the various advantages offered by VLSI in designing DSP Processors. (8)

22. a) Using DFT and IDFT determine the sequences $x_3(n)$ corresponding to the circular convolution of the sequences $x_1(n) = \{1,2,3,1\}$ and $x_2(n) = \{4,3,2,2\}$. (16)

(OR)

22 b)(i) Determine the fourier transform of the sequence

$$x(n) = 1 \text{ if } n \leq 0 \leq n_0 \\ = 0 \text{ otherwise}$$

and for $n_0=0$ what is $X(e^{j\omega T})$ (8)

(ii) Show that the EDCT is suitable for Image coding (8)

23. a) Design a chebyshev lowpass digital filter satisfying the specifications. (16)

Sampling time = 1 sec

Passband frequency = 0.06π rad/sec

Stopband frequency = 0.75π rad/sec

Passband attenuation = 6dB

Stopband attenuation = 20dB

(OR)

23 b) (i) Derive the time domain and frequency domain relations for the sampling rate conversion by a rational factor. (8)

(ii) Explain how round off noise is measured (8)

24 a) Explain in detail how the matrix and vector operations are implemented using Systolic arrays and Wavefront arrays. Compare them. (16)

(OR)

24 b) (i) Describe multi processor and multi computers architecture for DSP systems. (8)

(ii) Explain the various functions of PEs in DSP. (8)

25.(a) Explain the distributed arithmetic algorithm with an example and List its advantages (16)

(OR)

25 (b) What are the advantages of Bit serial arithmetic and explain how the it can be implemented using serial/Parallel multiplier. (16)
