Register Number .....

M.E DEGREE EXAMINATIONS: OCTOBER / NOVEMBER-2008

Second Semester

APPLIED ELECTRONICS

P07AEE11 – Low Power VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (20 x 2 = 40 Marks)

1. The power dissipated in charging and discharging load capacitance is
   A) Short-circuit power B) leakage power C) switching power D) capacitive power
2. Major sources of dynamic power are
   A) subthreshold and junction leakage current B) capacitive and short-circuit current
   C) subthreshold and short-circuit current D) capacitive and junction leakage current
3. In MOSFETs, methods of using implants control
   A) body effect B) reverse short-channel effect
   C) forward short-channel effect D) punchthrough
4. The subthreshold leakage current in CMOS digital circuit is reduced by
   A) transistor slicing B) charge sharing C) coding methods D) floorplanning
5. A 32 bit off-chip bus operating at 5V and 66MHz clock rate is driving a capacitance of 25pF/bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. The power dissipated in operating the bus is
   A) 41.25mW B) 132mW C) 165mW D) 330mW
6. Transistor sizing is a _____ optimization technique
   A) circuit level B) logic level C) behavioral level D) algorithm level
7. State assignment algorithm minimizes
   A) transition activity B) leakage current C) fan out D) area
8. Sufficient large aspect ratio minimize
   A) Short-channel effect B) Drain-Induced barrier-lowering effect
   C) Gate-Induced drain leakage effect D) Narrow-width effect
9. The number of logic gates from the signal node to a primary input is
   A) fan in B) glitches C) throughput D) logic depth
10. The energy efficiency of static CMOS is _____ of operating frequency.
    A) square B) inverse C) square root D) independent
11. Power saving techniques for flip-flops mostly concentrate on
    A) data energy B) clock energy C) switching energy D) signal activity
12. The phenomenon of randomly upset bits in a memory core is
    A) soft error rate B) activity factor C) bit rate D) bit line
13. The difference between signal required time and the signal arrival time at the output of a gate is
    A) intrinsic delay B) slack time C) signal delay D) dynamic time
14. The probability that a signal is at logic 1 is
    A) static probability B) conditional probability C) signal probability D) transition probability
15. Demerit of simulation based gate-level analysis is
    A) internal power B) capacitive power dissipation
    C) switching energy D) signal glitches

16. Entropy is related to
A) load capacitance B) operating frequency C) average power D) switching activity

17. Energy dissipated as a result of the processor switching from execution of one type of instruction to another is
A) base cost B) circuit state effect C) access cost D) instruction packing

18. Major improvements in power dissipation are possible at
A) behavioral level B) logic level C) circuit level D) gate level

19. Guarded evaluation is a technique to
A) reduce hardware resources by sharing long data buses with time multiplexing
B) reduce switching activity by adding pipeline register
C) reduce switching activity by adding latches
D) lower operating frequency

20. Event driven logic simulation is a
A) gate-level analysis B) switch-level analysis
C) circuit-level analysis D) architecture level analysis

PART B (5 x 12 = 60 Marks)

21. (a) Explain different components of power dissipation in CMOS VLSI circuits.

(OR)

(b) Explain various limiting factors in detail for low power VLSI design.

22. (a) Explain in detail, how power efficiency is achieved by network restructuring and reorganization

(OR)

(b) Explain logic level optimization for low power in detail.

23. (a) Discuss on adiabatic logic and power efficiency realized in adiabatic logic circuits over static CMOS logic circuits.

(OR)

(b) Explain low power techniques for SRAM.

24. (a) Explain the average power estimation in combinational and sequential circuits using statistical techniques with examples.

(OR)

(b) Discuss the effect of data correlation in power dissipation of VLSI circuits. Discuss a power analysis technique for a two input one output circuit based on signal correlation.

25. (a) Explain how software optimizations are useful for minimizing power in logic circuits.

(OR)

(b) Discuss power optimization by
(i) operation reduction.
(ii) Operation substitution.
(iii) Precomputation.

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