Register Number: .....

M.E. DEGREE EXAMINATION: OCTOBER/NOVEMBER-2008

Third Semester

APPLIED ELECTRONICS

P07AEE14-Computer Aided Design of VLSI Circuits

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions: -

PART A (20 × 1 = 20 Marks)

1. Logic synthesis is concerned with
   A) Optimization of circuit at the level of Boolean sets
   B) Optimization of circuit at the level of transistor
   C) Optimization of circuit at the level of layout
   D) Optimization of circuit at the level of fabrication steps

2. A graph that can be drawn on a two dimensional plane without any of its edges intersecting is called
   A) Planar B) Non planar C) Co-planar D) 2D plane

3. Time complexity of depth-first search is,
   A) O(n+Mod(E)), B) n(O+ Mod(E)) C) n+(Mod(O)+E) D)Mod(n)+E

4. Tractable problems are,
   A) Solved in polynomial time B) Solved in exponential time
   C) Solved in discrete time D) Solved in continues time

5. Stretchable rectangles correspond to
   A) Transistor B) Contact cuts C) Wires D) Diffusion

6. Directed acyclic graph has
   A) One cycle B) Two cycle C) No cycle D) Half cycle

7. Graph with edges never connect vertices of the same type and neither do they connect nets with cells is called
   A) Tripartite graph B) Hyper graph C) Bipartite graph D) Clique model

8. The Bellman – Ford algorithm is a
   A) Longest path algorithm B) Placement algorithm
   C) Compaction algorithm D) Partitioning algorithm

9. Wires that cross a cell without the wire necessary carrying a signal relevant the cell are called as
   A) By pass wire B) Jumpers C) Feedthrough Wires D) Connectors

10. If 'h' is the height of the cell, 'w' is the width 'A' is the area, whichever shape of the cell, h & w satisfy the Constraint

A)$hA \geq w$ B) $hw \leq A$ C) $hw < A$ D) $hw \geq A$

11. In channel routing the use of doglegs is,

A) To reduce channel height
B) To reduce channel width
C) To reduce channel area
D) To reduce channel height & width

12. Global routing concentrates on

A) Area and timing constraint
B) Only timing constraint
C) Height and timing constraint
D) Clocking constraint

13. An alternative method to the sum of minterm is

A) Two level logic synthesis
B) Binary-decision diagram
C) Product of sum
D) Canonical form

14. Registry transfer level (RTL) simulation is used in

A) Synchronous circuits
B) Asynchronous
C) Combinational circuits
D) Both synchronous & combinational circuit

15. Multigraph is a graph in which,

A) Parallel edges are allowed
B) Vertical edges allowed
C) Both parallel & vertical edges are allowed
D) Multiple edges are allowed from all the directions

16. If 'n 'switching stages given the switching delay is calculated as,

A) nRC B) n+RC C)$(RC)^n$ D) n^2 RC

17. Atomic nodes are used to perform

A) Addition, Subtraction & Multiply operation
B) Input and output operation
C) Relational operation
D) Storage operation

18. Synthesis of DFG is easier one if

A) DFG is transformed into an acyclic graph
B) DFG is transformed into parallelism mode with different interaction
C) DFG is transformed into software pipelining scheduling
D) High level transformations are used

19. Optimization of hardware unit Consisting of

A) Only speed & power consumption
B) Speed, area & power consumption
C) Speed, Cost, area & power consumption
D) Reduction of presence of capacitance effect

20. Retiming is for

A) Optimize the critical path of the DFG
B) Optimize the hardware unit
C) Overlapped scheduling
D) Optimize the floor planning method

PART B (5×16 =80 marks)

21. a)i)Write an algorithm for finding the shortest path in graphs and explain with examples (10)

ii)Discuss any three VLSI design automation tools used for physical design. (6)

(OR)

b) Explain the techniques for finding the optimal solution of a combinational optimization problem (16)

22. a) Explain kernighan –lin partitioning algorithm with suitable example (16)

(OR)

b)i) Explain liao-wang algorithm for the computation of longest path in directed graph (12)

ii) What are the types of minimum distance rule? (4)

23. a)i) Illustrate the various phases of the robust channel routing algorithm (10)

ii)What are difference between area, channel & global routing methods (6)

(OR)

b)i) Explain different floor planning concepts using slicing tree and wheel Floorplan method (8)

ii)Explain the necessity of shape functions related to floor planning (8)

24. a)i) Analyze zero-delay simulation, unit delay simulation and Pseudo code of full adder circuit using Compiler –driven simulation (10)

ii)Explain switch level modeling of a static NAND gate using a static CMOS, nMOS and CMOS domino logic (6)

(OR)

b)i) What is binary decision diagram? Explain how OBDD is transformed in to ROBDD using suitable Boolean function (10)

ii)List and explain the steps involved in two level logic optimization (6)

25. a)i) Explain date flow graphs (DFG) for simple date flow, contional date flow, iterative date flow with examples (8)

ii) Explain any one of scheduling algorithm for simple DFG (8)

(OR)

b)i) Explain how assignment can be done using clique partitioning (8)

ii) Explain about high level transformation from the associativity and distributivity law transformations (8)

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