Register Number.....

M.E. DEGREE EXAMINATIONS: DECEMBER 2009

First Semester

APPLIED ELECTRONICS

ANE501: Advanced Digital System Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL Questions:-

PART A (10 x 2 = 20 Marks)

1. Differentiate transition table and excitation table.
2. Draw the block diagram of synchronous clocked sequential circuit.
3. What is a race condition in flip flop? How it is eliminated?
4. Bring out a significant difference between Latch and Flip flop.
5. Draw the general structure of PLDS.
6. State Shannon's expansion theorem.
7. List the two types of experiments performed in testing?
8. Mention the algorithm for path sensation approach.
9. Write down the general syntax for the case statement in VHDL.
10. What is elaboration?

PART B (5 x 16 = 80 Marks)

11. a) i) Design a comparator which compares two n-bit binary number. Discuss the state table and logical implementation. (10)

ii) Discuss the general model of an Algorithmic State Machine (ASM). (6)

(OR)

b) i) Design a sequential circuit with four flips flops ABCD. The next states of B, C, D are equal to the present states of A, B, C. The next state of A is equal to the ex-OR of the present states of C and D. Discuss the state table and steps for such a logical design.

12. a) Design an Asynchronous sequential circuit with two inputs 'x ' and'y' and one output 'z'. Whenever 'y' is '1' input'x' is transferred to 'z'. When 'y' is '0' the output does not change for any change in 'x'. Draw the state transition diagram and using merger graph obtain the reduced flow table, and transition table.

(OR)

b) Design an Asynchronous sequential circuit which has two internal states and one ou the excitation and output function describing the circuit is given below:

$Y1=X1X2 + X1Y2 + X2Y1$

$Y2=X2 + X1Y1Y2 + X1Y1$

$Z=X2 + Y1$

13. a) Implement the following Boolean function using 8:1 multiplexer.

$F(A, B, C, D) = \prod M(0, 3, 5, 8, 9, 10, 12, 14)$

Discuss the implementation steps involved.

(OR)

b) Implement the following Boolean functions using 3 x 4 x 2 PLA and discuss t implementation steps with k-maps and PLA table.

$F1(a2, a1, a0) = \sum M(0, 1, 3, 5)$

$F2(a2, a1, a0) = \sum M(3, 5, 7)$

14. a) i) Discuss any three properties of Foldable Compatibility Matrix(FCM). (6

ii) Discuss the definition and theorem associated with COMPACT algorithm in derivin an FCM. (10

(OR)

b) i) Briefly discuss the types of faults in PLA. (8)

ii) Write a short note on signature Analysis. (8)

15. a) i) Model a D flip Flop using VHDL (4)

ii) Using the state graph, discuss the behavioral VHDL model for 4 x 4 binary multiplier. (12)

(OR)

b) Discuss the data path CPU design using VHDL for a simple microprocessor.

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