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M.E. DEGREE EXAMINATIONS: NOVEMBER 2009

Third Semester

APPLIED ELECTRONICS

P07AEE11 Low Power VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer ALL questions:-

PART A (10 x 2 = 20 Marks)

1. Give the expression for the current in the sub threshold region.
2. What is meant by static power dissipation?
3. What is meant by guarded evaluation?
4. Draw circuit diagram for true single phase clocked half latch.
5. What are the different phases used for adiabatic logic?
6. What is meant by clock gating?
7. Draw the diagram for circuit level representation of a transistor.
8. Give the simple power model for an adder circuit based on activities
9. What is the static power modes used in power PC system?
10. Define circuit state effects.

PART B (5 x 16 = 80 Marks)

11. (a) (i) Explain the sources of leakage power in CMOS circuits. (8)

(ii) Explain the sources of static power dissipation with an example. (8)

(OR)

(b) (i) Discuss the basic principles of low power design . (8)

(ii) Explain the components of node capacitance . (8)

12. (a) (i) Design of full adder using DRDL logic. (8)

(ii) Explain the local transformation operators for gate reorganization. (8)

(OR)

(b) (i) Design of full adder using SDCVSL logic . (10)

(ii) Explain Bus invert encoding. (6)

13. (a) (i) What is Boolean decision diagram and obtain BDD for Y = AB+BC+AC and its multiplexer implementation. (10)

(ii) Explain the pass transistor logic synthesis system. (6)

(OR)

(b) (i) Explain the low swing bus. (8)

(ii) Derive the power efficiency of adiabatic logic circuits. (8)

14. (a) (i) Discuss the power estimation using entropy analysis. (10)

(ii) Compute the transition density and static probability of Y=AB+C. (6)
given P (A) = 0.3,P (B) =0.4,P (C) =0.4,D(A)=1,D(B)=2,D(C)=3.

(OR)

(b) Explain the methods of gate level logic simulation for power estimation in VLSI circuits. (16)

15. (a) Write short notes on:

(i) Precomputation based optimization for low power. (10)

(ii) Power optimization using operation reduction. (6)

(OR)

(b) Explain in detail the software optimization for minimum power. (16)

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