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B.E. DEGREE EXAMINATIONS: NOVEMBER 2009

Fifth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U07EE505: Digital Logic Circuits

Time: Three Hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (10 × 1 = 10 Marks)

1. How many binary numbers are required to represent the decimal number $(17)_{10}$

   A. 3 B. 5 C. 4 D. 2

2. Union law states that _____

   A. A.A=A B. A.0=0 C. A.0=A D. A+A=A

3. In a 3-bit even parity generator, the output even parity bit for the input data 011 is _____

   A. 1 B. 0 C. 2 D. 3

4. The BCD output of the converter for Excess 3 input 1100 is _____

   A. 1001 B. 1111 C. 0011 D. 1100

5. The storage elements used in clocked sequential circuits are called _____.

   A. Counters B. Latch C. State D. Flip-flops

6. In flip-flops, the multiple transitions in the output observed in a single clock is called _____

   A. Race around condition B. Toggle C. Hazard D. Trigger condition

7. In asynchronous sequential circuit when the inputs and outputs are represented by pulses, then it is called_____

   A. Fundamental mode B. Pulse mode C. Trigger mode D. Transition mode

8. The state transition is directed through a unique sequence of unstable state variable change. This is referred to as _____

   A. Race B. Cycle C. Pulse mode D. State change

9. The number inputs that a logic gate can have _____

   A. Fan In B. Source In C. Source Out D. Fan Out

10. The P-channel MOS conducts when its gate to source voltage is _____.

    A. Positive B. Zero C. +5V D. Negative

PART B (10 x 2 = 20 Marks)

11. Find the 2's complement of 0101100.

12. Draw the circuit for OR logic function using NAND gates only.

13. Give the truth table for half subtractor.

14. What is decoder?

15. Mention the different types of triggering of flip-flops.

16. If a ring counter consists of 12 flip-flops, what is the maximum count capability?

17. Define critical race.

18. What is flow table?

19. Draw the inverter circuit using n-channel MOS logic circuits.

20. What is PAL?

PART C (5 x 14 = 70 Marks)

21. (a) (i). Perform the subtraction 3571 – 2101 using (1) 10's complement (2) 9's complement

(ii). Express the Boolean function F = x + y'z in a sum of product (sum of minterms) form.

(OR)

(b) Simplify the Boolean function F = ABCD + AB'C'D'+AB'C+AB using four variable K-map.

22. (a) (i). Design a full adder using 8:1 multiplier

(ii). Simplify the half adder truth table using K-map and implement using X-OR gate.

(OR)

(b) Design a 4-bit binary to gray code converter and implement using X-OR gate.

23. (a) (i). A logic circuits having a single input labeled X, and two outputs Y1 and Y2 is shown belo Investigate the circuit and find out does this circuit represents a latch? If yes, then name t latch and draw the truth table for this circuit. **FIGURE 1**

(ii) Explain the construction of clocked SR flip-flop with truth table.

(OR)

(b) Construct Ring counter using JK flip-flops and explain its operation with releva waveforms. Also explain any one of its application.

24. (a) Explain about fundamental mode circuit with latches and pulse mode operation of asynchronous sequential circuits.

(OR)

(b) Design an asynchronous sequential circuit that has the output Y which must remain 0 as lo as one of its inputs X_1 is 0. While $X_1 = 1$, the occurrence of first change in another input X_2 should give Y = 1 as long as $X_1 = 1$ and becomes 0 where X_1 returns to 0.

5. **(a)** (i). Implement the following function using 3-input, 3 product terms and 2 output PLA (7)

$F_1 = AB' + AC = \Sigma(4, 5, 7)$

$F_2 = AC + BC = \Sigma(3, 5, 7)$

(ii) Explain the working of a 3 input Totem pole NAND gate. (7)

(OR)

(b) Explain the architecture of FPGA with neat diagram and also give its applications.

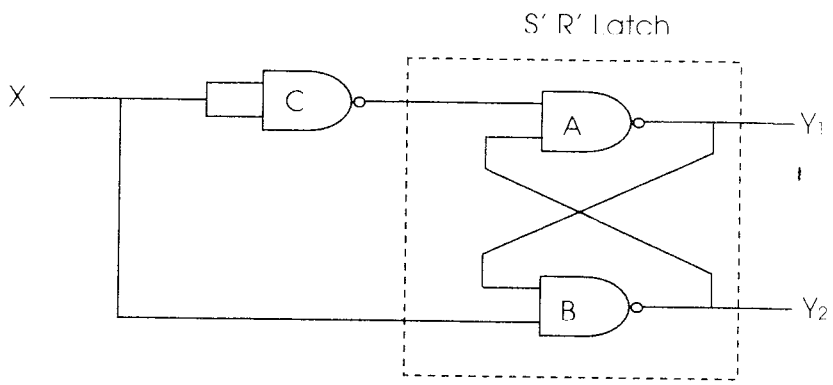

FIGURE 1

Q. 23 (a) (i)

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