Register Number .....

B.E. DEGREE EXAMINATIONS: NOVEMBER 2009

Third Semester

MECHATRONICS ENGINEERING

U07MH303: Digital Electronics

e hours **Maximum Marks: 100**

Answer ALL the Questions:-

PART A (10 x 1 = 10 Marks)

t the following decimal number to their hexadecimal equivalent 62.500_{10}

a) $(3E.8)_{16}$ b) $(391)_{16}$ c) $(3E.1)_{16}$ d) 3E1

ify the following expression $Z = (\overline{A} + B)(A + B)$

a) z=1 b) z=0 c) z=B d) z=A

_____ n inputs produce 2^n outputs.

a) Encoder b) Multiplexer c) Decoder d) Demultiplexer

PAL has programmable for connections for the _____ gates

a) OR b) AND c) NOT d) NAND

What is the characteristics equation of JK FLIP-FLOP?

a) $Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$ b) $Q_{n+1} = J Q_n + K\overline{Q_n}$

c) $\overline{Q}_{n+1} = \overline{J}\ \overline{Q_n} + K\ Q_n$ d) $Q_{n+1} = JQ_n + \overline{K}\ \overline{Q_n}$

A flash memory behaves as a _____ RAM

a) Non-Volatile b) Volatile c) Erasable d) Masked

7. A minimum number of _____ changes must occur in the output corresponding to dynamic hazard

a) Three b) One c) Four d) Two

8. A ripple counter is _____ circuit.

a) Synchronous sequential b) Asynchronous sequential

c) CombinationalCircuits d) Transistor Circuits.

9. 0 / 1 written by the side of a directed arc in a state diagram indicates 0 _____ and 1 _____

a) Input,Output b) Output, Input c) Input, Input d) Output,Output

10. A Programmable logic array has a programmable _____ array whose product term output feed a programmable _____ array.

a) OR, AND b) NOR, AND c) AND, OR d) NAND, NOR

PART B (10 x 2 = 20 Marks)

11. What is the procedure to simplify the Boolean expression by K-map?
12. What are Minterms and Maxterms?
13. Distinguish between decoder & de-multiplexer
14. What is mean by access time of a memory?
15. Convert SR and JK flip-flop into D-flip-flop.
16. How does ROM retain information?
17. What is meant by Race?
18. Mention any one advantages and disadvantages of asynchronous sequential Circuit.
19. What are the basic elements of ASM chart?
20. What is the advantage of one-hot design method?

PART C (5 X 14 = 70 Marks)

21 (a) Verify the following equation by using Boolean algebra

i) $AB+AC+\overline{B}C = AC+\overline{B}\,\overline{C}$ (6)

ii) Simplify the following expression $(AB+C+D)(\overline{C}+D)(\overline{C}+D+E)$ (8)

(OR)

(b) Implement the switching function whose octal designation is 274 using NOR gates only.

22 (a) (i) Construct a 4-bit adder with carry lookahead scheme.

(ii) Construct a 4 to 16 line decoder with five 2 to 4 line decoder with enable.

(OR)

(b) (i) Design an 8-bit BCD adder using IC 74283 (10)

(ii) Implement the following Boolean function with 8:1 multiplexer.

$F(A,B,C,D) = \Pi M(0,3,5,6,8,9,10,12,14)$. (4)

23 (a) Design a synchronous counter that goes through the sequence 2, 6, 1,7,5,4 and repeat use JK flip-flop

(OR)

(b) With the help of two shift register design a 4-bit serial adder.

ment the switching function f=∑(1,3,5,7,8,9,14,15) by a static hazard free two AND-OR gate network?

(OR)

n Synchronous sequence circuit is described by the following excitation and tput function $B=(\overline{A_1}+B_2)\,B+(A_1+B_2)$ and $C=B$

(1) Draw the logic circuit (5)

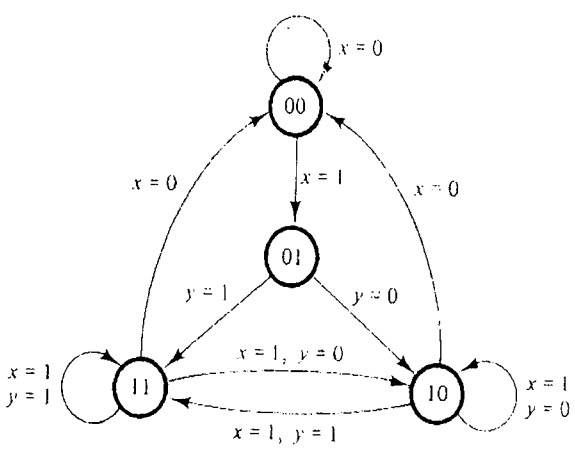
(2) Draw the transition table and output map (5)

(3) Describe the behavior of the circuit (4)

) Draw (1) a block diagram showing the controller, datapath unit (with internal registers), and signals, and (s) the portion of an ASMD chart starting from an initial state. There are two control signals: x and y. If xy = 01, register R is incremented by 1 and control goes to a second state. If xy = 10, register R is cleared to zero and control goes from the initial state to a third state. If xy=11, register R is decremented by 1 and control goes to fourth state. Otherwise,control stays in the initial state. Assume active-low synchronous reset.

(OR)

(b) Draw the equivalent ASM chart for the given state diagram of a control unit, it has 4-states and two inputs x and y.



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