Q 8013

M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

First Semester

Applied Electronics

AN 1602/ ES 1601 — ADVANCED DIGITAL SYSTEM DESIGN

(Common to M.E. VLSI Design and M.E. Embedded System Technologies)

(Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the steps involved in the design process of synchronous sequential systems.

2. Draw the ASM Diagram for the mealy model with one input x and one output z such that z = 1 iff x has been 1 for three consecutive clock times.

3. What are the two modes of operation of asynchronous sequential machines?

4. State the most important consideration in making state assignments for asynchronous networks.

5. State the conditions for two faults to be equivalent and the condition for a fault to be Redundant.

6. Define a test vector.

7. Draw the FPGA design Flow.

8. Draw the internal structure of a Complex PLD.

9. What are guarded signals?

10. State the syntax rule for procedure declaration in VHDL.

11. (i) Explain the process of designing a synchronous sequential circuit using a GAL. (8)

    (ii) Describe in detail the internal structure of FPGA. (8)

12. (a) For each of the following circuits and input strings.

    (i) Construct a state table (calling the state 00, 01, 10, 11) and show a timing trace for the values of the flip-flops and the output for as far as possible. Assume that the initial value of each flip-flop is zero. (8)

    (ii) For the following circuit and input string construct a state table (calling the states 00, 01, 10, 11) and show a timing trace for the values of the flipflops and output as far as possible. Assume that the initial value of each flipflop is zero. (8)


clock   X : 001100110
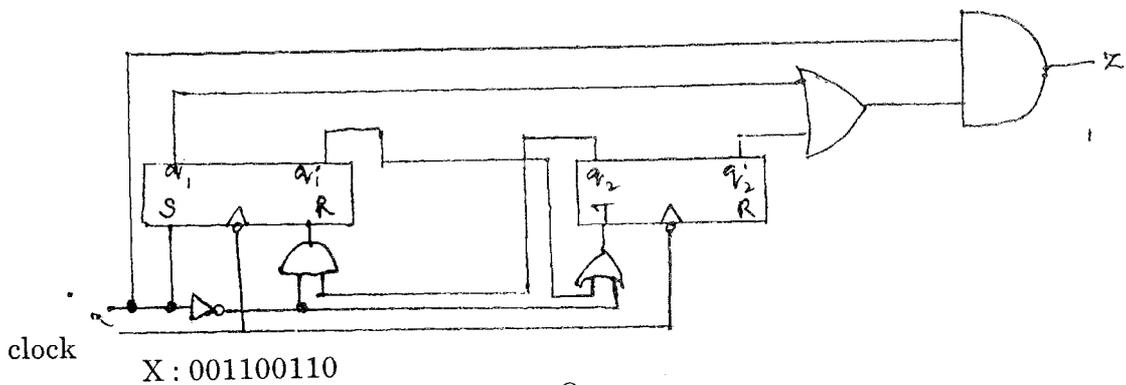
Or

    (b) (i) Design a counter that goes through the following sequence of states that are not in numeric order.

    0, 3, 2, 4, 1, 5, 7 and repeat (8)

    (ii) Design a mealy system whose output is 1 iff there have been exactly two one's followed by a 0 and then a 1. (8)

        (1) Assume overlapping is allowed.

        (2) Assuming overlapping is not allowed.

13. (a) An inhibited toggle Flipflop has a trigger input, T, and inhibit inputs, I_0 and I_1. The Flipflop output (Q) will change state if $I_0 = 1$ when T changes from 0 to 1, or if $I_1 = 1$ when T changes from 1 to 0. The Flipflop will not change state at any other conditions. You may assume that I_0 and I_1 will always be constant when T is changing.

    (i) Find a minimum-row flow table for the flipflop (4 rows). (List the input variables in the order T, I_0, I_1.) (4)

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(ii) Design the Flipflop using NAND Gates and inverters only. First design the network without eliminating hazards. Using your flow table and maps, indicate how one of the static hazards can cause the network to go the wrong state. For this hazard, indicate the order in which the gates must change for the hazard to actually show up. (6)

(iii) Add the necessary gates to the network designed in part 2 to eliminate the combinational logic hazards.

I_0 ——▶ | Inhibited Toggle Flipflop | ——▶
I_1 ——▶
T ——▶

(6)
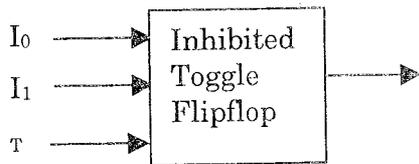
Or

(b) Find a hazard free realization for each of the following functions using only three input NOR gates

(i) $f(a, b, c, d) = \Sigma\, m(0, 2, 6, 7, 8, 10, 13)$ (8)

(ii) $f(a, b, c, d) = \Sigma\, m(2, 3, 6, 7, 8, 10, 13)$ (8)

14. (a) (i) Explain the path sensitization method. (5)

(ii) Derive by path sensitization method the test vectors for the SA0 and the SA1 faults at g and h in the network of the following figure. (11)

Or

(b) Describe in detail Fault tolerance techniques and fault tolerant VLSI processor arrays.

15. (a) With diagrams explain the process of designing a simple microprocessor using VHDL.

Or

(b) Write the VHDL code for Serial Adder, Binary multiplier and Binary divider.

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