# Q 8019

M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

*Elective*

Applied Electronics/VLSI Design

AN 1625 — ASIC DESIGN

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the steps to construct any single–stage combinational CMOS logic cell.

2. Define "Logical Effort" and "Electrical Effort".

3. Give the names of any four benchmark circuits of PREP.

4. What does "Speed Grading" mean?

5. What are the ways to perform "logic minimization"?

6. What are the terms used in Circuit Schematics?

7. What are the common encoding options of Finite State Machine?

8. What are the differences between "Compiled Code Simulation" and "Native Code Simulation"?

9. What are the Goals and Objectives of Global Routing and Detailed Routing?

10. Define "Channel Allocation".

PART B — (5 × 16 = 80 marks)

11. (i) What does ASIC Design Flow mean? List the salient features of each stage of ASIC Design Flow. (8)

(ii) Construct two–input NAND and two–input NOR logic gates using CMOS Logic Cell. (8)

12. (a) (i) What is meant by "Antifuse"? Explain the process of Metal–metal Antifuse. (8)

(ii) Explain the Static RAM Programming Technology with an example. (8)

Or

(b) (i) Explain how Multiplexer Logic used as Function Generator. (8)

(ii) Explain how Shannon's expansion theorem is used to expand Boolean logic function in terms of Boolean variable. (8)

13. (a) (i) How do you measure the delay of a net using an RC Tree? (8)

(ii) Explain the Hierarchical Design with Schematic example. (8)

Or

(b) (i) Explain how to construct 4–bit latch using complex sub–schematic. (8)

(ii) How do you use "Bus" to simplify a schematic? (8)

14. (a) (i) Explain the Logic Synthesis with an example. (8)

(ii) Describe the process of Gate level Simulation. (8)

Or

(b) (i) Discuss the salient features of Boundary Scan Test. (8)

(ii) Explain the different features of Stuck–at Fault Model. (8)

15. (a) Write short notes on :

(i) System partitioning. (8)

(ii) Estimating ASIC Size. (8)

Or

(b) Write short notes on :

(i) Floorplanning tools. (8)

(ii) Global routing between blocks. (8)