Q 8024

M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

Second Semester

Applied Electronics

AN 1651 — ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Common to M.E. Computer and Communication and M.E. VLSI Design)

(Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

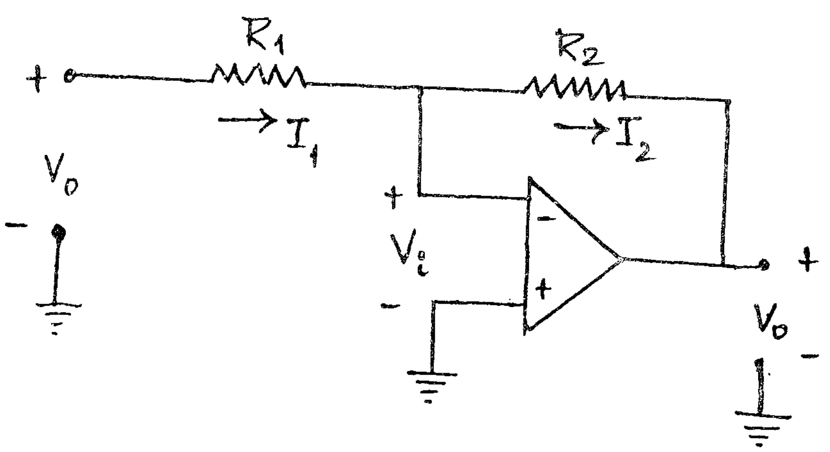
1. What is meant by weak inversion in MOS transistor?

2. How does substrate voltage affect the VI characteristics of MOSFET?

3. What is the main difference between current source and current sink?

4. What is an bootstrap reference?

5. Calculate the gain of the circuit for a open loop gain of 10^4 and $R_1 = 1\,K\Omega$, $R_2 = 10\,K\Omega$.



6. What is an miller capacitance? Also give the expression.

7. Draw the circuit of a simple emitter coupled pair multiplier.

8. Write the difference between the analog multiplier and four quadrant multiplier.

9. List any two high output impedance current mirrors and their advantages.

10. How the input common-mode range and power-supply rejection of the two-stage operational Amplifier are improved?

PART B — (5 × 16 = 80 marks)

11. (i) For an Op Amp model with two poles and one right half plane (RHP) zero, prove that if the zero is ten times, higher than unity gain bandwidth (GB), then in order to achieve a 60° phase margin, the second pole must be placed at least 2.2 times higher than unity Gain Bandwidth. (GB) (10)

(ii) Explain the simplified version of an n-channel input, folded cascode Op Amp. (6)

12. (a) (i) Derive the depth of depletion region of a Pn Junction. (8)

(ii) An abrupt Pn junction in silicon has doping densities $N_A = 10^{15}$ atoms/cm^3 and $N_D = 10^{16}$ atoms/cm^3. Calculate the junction built-in potential, the depletion-layer depths and the maximum field with 10 V reverse bias. (8)

Or

(b) Derive the complete small-signal model for an NMOS transistor with $I_D = 100\mu A$, $V_{SB} = 2V$, $V_{DS} = 5V$. Device parameters are $\phi_f = 0.3$ V, $W = 30\mu$, $L = 10\mu$, $\gamma = 0.5V^{1/2}$, $K' = 16\mu A/V^2$, $\lambda = 0.02V^{-1}$, $t_{OX} = 0.1\mu$, $\psi_0 = 0.6V$, $C_{sbo} = C_{dbo} = 0.1$ pF. Overlap capacitance from gate to source and gate to drain is 0.01 pF. Assume $C_{gb} = 0.05$ pF. (16)

13. (a) (i) Derive the small signal output resistance of a current source and current sink. (8)

(ii) Explain in detail about the general principle of the bandgap reference. (8)

Or

(b) (i) Compare the Emitter follower, source follower and push-pull output stages. (6)

(ii) Discuss the techniques involved in the design of temperature independent biasing methodologies. (10)

14. (a) (i) Explain in detail about the miller compensation of the Two-stage Op Amp. (8)

(ii) Derive the frequency response of an Operational Amplifier. (8)

Or

(b) Explain in detail about the

(i) Positive Power-Supply Rejection Ratio and Negative Power-Supply Rejection Ratio of two stage Op Amps. (6)

(ii) High frequency analysis of operational amplifier. (10)

15. (a) (i) Explain the Gilbert Multiplier Cell in detail. (8)

(ii) Give the dc analysis of the Gilbert multiplier cell. (8)

Or

(b) (i) With block diagram explain the PLL system. (6)

(ii) A PLL has a VCO gain K_o of 2π (1 kHz/V), a loop bandwidth K_v of 500 S^{-1}, and a free-running frequency of 500 Hz.

(1) for a constant input signal frequency of 250 Hz and 1 kHz, find V_o.

(2) Now the input signal is frequency modulated, so that

$w_i(t) = (2\pi)$ 500 Hz $[1 + 0.1 \sin(2\pi \times 10^2)t]$. Find the output signal $V_o(t)$. (10)

———————