M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

Second Semester

Applied Electronics/VLSI Design/Computer and Communication

AN 1652 — COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(Regulation 2005)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the formula for efficiency of linear pipline.

2. What is memory interleaving?

3. Give any two conditions of parallelism.

4. Compare control flow and data flow computing

5. Draw the PRAM model of parallel computation.

6. Differentiate between multiprocessor systems and multi computer systems.

7. Name any two programming languages that support parallel programming.

8. What is the difference between UMA and NUMA multiprocessors?

9. What is the principle of fine grain multi computers?

10. What is the difference between a binary k-cube and cube connected network of degree k?

PART B — (5 × 16 = 80 marks)

11. (i)   Given a task that can be divided into m subtasks, each requiring 1 unit of time, how much time is required for an m-stage pipeline to process n tasks?   (4)

    (ii) Summarize the similarities and differences between RAM model of serial computation and PRAM model of parallel computation.   (8)

    (iii) Define the Amdahl's law of speed up.   (4)

12. (a) (i) Let page trace $P = abacabdbacd$ if $|M_P| = 2$ page frames, What is the hit ratio for LRU, MRU and FIFO replacement algorithms? Also find the hit ratio for $|M_P| = 3$ page frames, using the above algorithms. (8)

(ii) Consider three inter leaved memory organizations for a main memory system containing 8 memory modules $M_0, M_1, \cdots M_7$. Each module has a capacity of $2K$ words. So the total memory capacity is $16\ K$ words. The maximum memory bandwidth is 8 words/cycle. In each of the following organizations, first specify the memory address (14 bits), them show the address assignment patterns in each memory module, and finally indicate the maximum bandwidth when one of the 8 modules fails to function :

(1) 8-way interleaved memory orgn. (one group)

(2) Grouped 4-way interleaved orgn. (two groups)

(3) Grouped 2-way inter leaved orgn. (four groups). (8)

Or

(b) (i) Explain how virtual address translation is done in segmented memory system. (10)

(ii) Enumerate the various page replacement policies. (6)

13. (a) (i) Compare linear and non-linear pipe line processors. (4)

(ii) Design an arithmetic pipeline for multiplying two 6 bit numbers. (12)

Or

(b) (i) Write about the design issues of super scalar and super pipeline. (8)

(ii) Explain the various message passing mechanisms in parallel architecture. (8)

14. (a) (i) Describe in detail the concept of compound vector processing. (8)

(ii) Explain the static data flow computer architecture. (8)

Or

(b) Write notes on :

(i) Multi vector Multi processors

(ii) Multithreading

(iii) Hybrid architectures. (16)

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15. (a) (i) Explain the MACH/OS Kernel architecture. (8)

(ii) Write about the parallel programming models. (8)

Or

(b) (i) Write about the programming languages that support parallel programming. (8)

(ii) Describe in detail about the OSF/1 architecture. (8)

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