

Q 8027

M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

Second Semester

Applied Electronics

AN 1654 - EMBEDDED SYSTEMS.

(Common to M.E. VLSI Design, M.E. Computer and Communication and
M.E. - Communication Systems)

(Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is Embedded Computer System?
2. Define UML.
3. What is RISC processor?
4. What is the purpose of CPSR in ARM processor?
5. What data type does the SHARC support?
6. How error is detected in CAN BUS?
7. What is CSMA / CD?
8. List out the five levels of maturity in CMM.
9. Define the function of RTOS.
10. What is a system - on - a chip?

PART B — (5 × 16 = 80 marks)

11. (i) Discuss the challenges in Embedded Computing system design. (8)
(ii) Explain in detail about the use of UML in Model train control system. (8)
12. (a) (i) Explain the difference between a big - endian and little endian data representation in ARM processor. (9)
(ii) Explain the various Logical and Arithmetic instructions available in ARM processor. (7)

Or

- (b) (i) Explain the complete design methodology of a 24-hour digital clock with a single alarm. (10)
(ii) Briefly explain Register-Indirect addressing and base-plus-offset addressing in ARM processor. (6)
13. (a) (i) Explain the memory organization in SHARC processor. (8)
(ii) Compare and contrast the off-line and on-line in scheduling. (8)

Or

- (b) (i) Describe the differences between the waterfall and spiral development models. (10)
(ii) Explain various quality assurance techniques. (6)
14. (a) (i) Explain the seven layers of OSI model. (6)
(ii) How messages are transmitted between microcontrollers using I²C bus? Explain. (10)

Or

- (b) (i) Write short notes on Internet based Embedded system. (8)
(ii) Explain the CAN Data frame format. (8)
15. (a) (i) Discuss the hardware and software architecture of SET-TOP box. (10)
(ii) Explain the weighted round robin approach in Real-time systems. (6)

Or

- (b) (i) Explain the system architecture of Telephone PBX. (8)
(ii) Describe the challenges in validating timing constraints in priority driven system. (8)