P 7029

M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

Second Semester

Applied Electronics

AX 141 — COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(Common to M.E. VLSI Design)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List out the policies adapted in CRCW–PRAM model to handle CW conflicts.

2. Compute the effective CPI of a computer, which is having a 10 MHz processor with MIPS rate of 15.

3. Define multicast.

4. Using Amdhal's law, show that the speed up is inversely proportional to fraction of sequential code in the program.

5. Define coherence property of memory.

6. A synchronous bus has a cycle time of 50 ns and each bus transmission take 1 clock cycle. The data portion of the bus is 32 bits (one word) wide. What is the bandwidth for the bus when performing one word reads from a 150 ns memory?

7. What is sequential consistence?

8. Consider a pipeline processor, which has 5 stages and takes 100 ns to execute n instructions. How long will it take to execute 2 n instructions, assuming the clock rate is 500 MHz?

9. Convert the following FORTRAN scalar loop into an equivalent one vector add instruction.

```
DO 20 I = 8, 120, 2
20 A (I) = B (I + 3) + C (I + 1)
```

10. Write any two difference between time sharing and space sharing operating systems.

PART B — (5 × 16 = 80 marks)

11. (i) Discuss the architecture of UMA, NUMA and COMA. (8)

(ii) What are the difference between SIMD and MIMD computers and explain any one in detail. (8)

12. (a) Explain the various static and dynamic architecture available for interconnecting computer subsystems.

Or

(b) Briefly explain grain packing mechanism for parallel programming applications. Discuss how the node duplication eliminates communication delays between the processors.

13. (a) Explain the implementation of direct mapping cache in a system having a cache size of 64 K and main memory size with 32 M bytes.

Or

(b) Discuss the following technique to achieve a collision free scheduling in the pipeline implementation.

(i) Collision vector. (4)

(ii) State diagrams. (3)

(iii) Single cycle. (3)

(iv) Greedy cycle. (3)

(v) MAL. (3)

14. (a) Discuss the snoopy protocol and directory based protocol in solving the multicache inconsistency problem.

Or

(b) Briefly explain how the pipeline chaining is used in cray 1 and cray X–MP by considering the following CVF $Y(1:N) = Sx\ X(1:N) + Y(1:N)$ and with the help of the timing diagram, show that the vector chaining in cray X–MP provides a best performance compared with cray 1.

15. (a) Briefly discuss the following synchronization methods used in solving the problem of shared objects in a concurrent processes.

(i) Mutual exclusion

(ii) Semaphores

(iii) Reader/writer locks

(iv) Monitors. $(4 \times 4 = 16)$

Or

(b) Briefly investigate the following methods for vectorization of scalar code by considering an example code of your choice.

(i) Vector reduction

(ii) Loop interchanging

(iii) Loop distribution

(iv) Node splitting. $(4 \times 4 = 16)$
