P 7430

M.E. DEGREE EXAMINATION, MAY/JUNE 2006.

VLSI Design

Elective

VL 034 – LOW POWER VLSI DESIGN

(Common to ME-Applied Electronics)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the need for low power VLSI chips.

2. Define static probability of a digital signal.

3. What is power management?

4. What are the sources of leakage power dissipation?

5. State and explain the terms of dynamic power dissipation equation.

6. What is overlap capacitance?

7. What is Glitching power?

8. What are finite-state machine?

9. State any four sources of software power optimisation.

10. Draw an adiabatic dynamic logic CMOS inverter.

PART B — (5 × 16 = 80 marks)

11. (i) Explain briefly the various software power optimisation techniques.   (10)

    (ii) Discuss the basic principles of lower design.   (6)

12. (a) Explain gate-level power analysis using simulation.

Or

(b) Explain :

(i) Architecture-level power analysis. (8)

(ii) Short-circuit current in CMOS circuit. (8)

13. (a) (i) Explain the transistor and gate sizing for power reduction. (8)

(ii) Explain the bus invert encoding. (8)

Or

(b) (i) What is the problem encountered by low power parallel multipliers? Suggest and explain a method to overcome it. (8)

(ii) Explain a low power high-speed SRAM cell. (8)

14. (a) Write notes on :

(i) Complementary adiabatic logic. (6)

(ii) Energy bands of a MIS structure under various biasing condition. (10)

Or

(b) Explain the long channel MOSFET and submicron MOSFET.

15. (a) Explain the estimation of average power in logic circuits using statistical techniques.

Or

(b) Explain the behavioural synthesis of circuits to achieve low power.

———————————