Z 3512

M.C.A. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Third Semester

MC 1702 — MICROPROCESSORS AND ITS APPLICATIONS

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the difference between a microprocessor and a microcontroller?

2. What do you mean by multiplexed address bus in 8085? What is the advantage of having these kinds of multiplexed buses?

3. What feature should be available in a microprocessor so that a microcomputer designer can use both memory mapped I/O and I/O mapped I/O?

4. If the DS register of 8086 contains 4000_h, what physical address will the instruction MOV AL, [2345_h] read?

5. Can the 8086 microprocessor operate on more than one instruction at a time? If so, explain how it is done.

6. Which signals are used by 8086 microprocessor to specify the current segment portion of the address referred?

7. Distinguish the real, protected and virtual modes of 80386.

8. What do you mean by inquire cycle in Pentium microprocessor? Explain its need.

9. What do you mean by leading-edge and trailing-edge problems in hexadecimal keyboards?

10. State any two main functions of a CRT controller.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the instruction cycle of 8085 with timing diagram. (6)

(ii) Explain the memory-IO read and memory-IO write cycles of 8085 with timing diagrams. (10)

Or

(b) (i) Discuss the architecture of DMA controlled data transfer in 8085 microprocessor with neat diagrams. (7)

(ii) What are the registers available in 8257 DMAC? What are their functions? (6)

(iii) Specify the advantages of DMA controlled data transfer over other modes of data transfer. (3)

12. (a) (i) Describe with a block diagram the internal architecture and working of all the internal units of a 8086 microprocessor. (10)

(ii) How many times does the NOP instruction execute in the following sequence of 8086 code? Also explain the working of this code. (6)

```
        MOV     CX,     20h
XYZ:    PUSH    CX
        MOV     CX,     09h
ABC:    NOP
        LOOP    ABC
        POP     CX
        LOOP    XYZ
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Or

(b) (i) With examples explain the different addressing modes supported in 8086. (7)

(ii) Assume that the DS register contains 0100_h and register SI contains 0020_h. Assume the data from 01020_h to 01023_h are 30_h, $F0_h$, 80_h and 90_h continuously. What is the result of executing the instruction LDS DI, [SI]? Give the contents of all the registers involved in executing this instruction. (3)

(iii) Explain the operation of the following instruction.

(1) LOOP

(2) JCXZ

(3) MUL CX. (6)

13. (a) (i) Explain the need for having two modes of operation of 8086. (3)

(ii) Describe the 8086 bus cycle with its timing diagram. (8)

(iii) The memory interfaced to the 8086 is a byte-organized memory. Explain this statement and also state how the signals A_0 and $\overline{BHE}$ are used in resolving the memory addresses. (5)

Or

(b) (i) Describe in detail how the different types of memories are interfaced with 8086. (8)

(ii) What is meant by polling? Explain the working of programmed I/O data transfer with respect to 8086 CPU. (8)

14. (a) (i) Show how the $M/\overline{IO}$ and $W/\overline{R}$ signals get decoded to generate MRDC, IORC and IOWC signals for interfacing memory and I/O to 80386 processor. (4)

(ii) Elaborate the design of memory used in 80386 based systems. (5)

(iii) Describe the salient features of 80386 processor. (7)

Or

(b) (i) With a block diagram explain the functional units of PENTIUM processor. (8)

(ii) List the salient features of PENTIUM that are not available in i80x86 machines. (4)

(iii) Explain why the address bus of PENTIUM is bidirectional. (4)

15. (a) (i) With a neat diagram explain how an LRC 7040 printer be connected to a microprocessor. (10)

(ii) Describe how the number 6 will be generated in LRC 7040 printer. (6)

Or

(b) (i) Elaborate the working of CRT display. (7)

(ii) Explain how characters are generated using a CRT controller. (3)

(iii) Discuss how the CRT controller is interfaced with the DMA controller and character generator ROMs for dot matrix decoding. (6)
