

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

Fifth Semester

Computer Science and Engineering

CS 334 — MICROPROCESSORS

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the types of instruction for 8085 microprocessor?
2. What are the addressing modes for 8085 microprocessor?
3. Why is an interrupt driven I/O more efficient than programmed I/O for 8086 microprocessor?
4. An interrupt device based on 8086 microprocessor sends $03H$ onto ADO thru AD7 data bus when \overline{INTA} is low. Where should the interrupt jump address located in the vector table?
5. Name the signals used by 8086 to demultiplex the address/data bus and to control the data bus buffers.
6. Name the software operation possible with the 8086 compared with 8085 microprocessor.
7. Name any two important methods available for error correction during serial communication.
8. What is meant by "baud - rates" and how is it achieved?
9. What is meant by dual - level cache memory in PENTIUM based system?
10. Name any four specification for PENTIUM processor.

PART B — (5 × 16 = 80 marks)

11. (i) Write an assembly language program based on 8085 (Eighty-five) microprocessor to implement a look-up table translation to generate the codes for seven-segment display with four digits. (Assume INPUT PORT $0D6H$, and OUTPUT PORT $0D4H$) (12)
- (ii) Name the four different ways of passing parameters in 8086 microprocessor to a procedure in assembly language. (4)

12. (a) (i) Write an 8085 assembly language program to perform 32 bit binary addition. (12)
- (ii) What will be the value in ACC, for the given 8085 program below :

```
MVI C, 7 F
MVI B, 3 E
MOV A, B
RLC
RLC
ANI 7 F
HLT.
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(4)

Or

- (b) (i) Write an 8085 assembly language program to fill a block of 1000_H bytes starting at address 9000_H with characters 2B_H. (12)
- (ii) Indicate the logic levels on each control or status pin as logic '0' or logic '1' for 8085 microprocessor with the given table below : (4)

Machine cycle	\overline{RD}	\overline{WR}	IO/\overline{M}	S 0	S 1
Memory write					
Memory read					
I/O write					
I/O read					
O/P code fetch					

13. (a) Write a brief note on 8086 based multiprocessor system design/configuration. (16)

Or

- (b) Write a brief note on 8086 based maximum mode and minimum mode CPU module with a neat diagram. (16)

14. (a) Explain in detail with a neat diagram, how 8259 (Programmable Interval Timer) can be used for interrupt generation and control. (16)

Or

- (b) What are the capabilities of 8251A-USART for asynchronous communication purposes? Explain its operation with a neat diagram. (16)

- (a) Explain the concept of pipelining for integer and floating point operation for PENTIUM processor with the help of neat diagram. (16)

Or

- (b) With a neat functional block diagram, explain for a PENTIUM processor
- (i) its capabilities and architecture. (12)
 - (ii) functional grouping of its pins. (2)
 - (iii) ways to address 64 bit, 32 bit, 16 bit and 8 bit memories in HARDWARE. (2)
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