B 265

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

Fourth Semester

Computer Science and Engineering

CS 238 — COMPUTER ARCHITECTURE — I

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is a load–store architecture? Discuss.
2. Explain the absolute and auto – increment addressing modes with an example instruction.
3. Discuss the IEEE format used for representing single – precision floating – point numbers.
4. Discuss the principle of operation of a carry save adder.
5. What are the advantages and disadvantages of hardwired and micro programmed control?
6. What is the ideal speedup expected in a pipelined architecture with 'n' stages? Justify your answer.
7. Distinguish between the write – through and write – back policies pointing out their relative merits and demerits.
8. What is an interleaved memory system? Discuss.
9. Distinguish between memory mapped I/O and I/O mapped I/O.
10. Consider a computer in which several devices are to be serviced interrupts. How do you handle this if the processor has only one interrupt request line?

PART B — (5 × 16 = 80 marks)

11. (i) Consider the following instruction :

ADD (RO) + , R1, (R2)

Where the first two are source operands and the third is the destination operand. Show the control sequence to execute this instruction for a single bus organization assuming the instruction itself is only a one word instruction. (8)

(ii) What are the features to be considered while designing the instruction formats of a processor? Discuss in detail. (8)

12. (a) (i) Discuss the principle of operation of carry look ahead adders. (4)

(ii) Design a 64 – bit adder that uses four 16–bit carry – look ahead adders along with additional logic to generate c16, c32, c48 and c64 from c0 and the G_i^{II} and P_i^{II} variables. Also calculate the delay for generating s63 and c64. (12)

Or

(b) (i) Discuss the operation of a floating point adder/subtractor unit. (12)

(ii) Simulate the addition operation on the operands :

A = 0 10001 011011

B = 1 01111 101010

With a five – bit signed excess – 15 exponent and a six – bit normalized fractional mantissa. (4)

13. (a) Give the organization of a typical hard wired control unit and explain the functions performed by the various blocks. Discuss the data flow for a sample instruction.

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome/minimize these hazards?

14. (a) (i) Discuss the various mapping techniques used in cache memories.(12)

(ii) A computer system has a main memory consisting of 1M words. It also has a 8K –word cache organized in the block – set – associative manner, with 4 blocks per set and 64 words per block.

Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format. (4)

Or

(b) (i) Explain the concept of virtual memory with any one virtual memory management techniques. (12)

(ii) Give the basic cell of an associative memory and explain its operation. (4)

(a) (i) What are the functions to be performed by a typical I/O interface?(4)

(ii) Explain the interrupt driven mode of data transfer and the DMA driven data transfer elaborating on how they are accomplished and their relative merits and demerits. (12)

Or

(b) Write short notes on the following : (2×8)

(i) Laser printers

(ii) Any two input devices.
