A 221

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

Third Semester

Computer Science and Engineering

CS 232 — DIGITAL SYSTEMS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State a single rule, which can be used to form the complement of a Boolean expression in one step.

2. Find the minterm expansion of $f(a, b, c, d) = a'(b' + d) + acd'$.

3. Define the following terms : implicant, prime implicant, essential prime implicant.

4. What size ROM is required to realize four functions of five variables?

5. What is meant by a functionally complete set of logic gates?

6. Is the PAL same as the PLA? Justify.

7. Explain how parity can be used for error detection.

8. What is iterative network?

9. Define a primitive flow table.

10. Define the following terms : race, critical race, non–critical race.

PART B — (5 × 16 = 80 marks)

11. (i) Simplify the following function using tabulation method. (12)

$$f(a, b, c, d) = \Sigma m\,(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d\,(4, 8, 11)$$

(ii) Design a combinational circuit whose input is 4 bit binary number and whose output is 2's complement of input number. (4)

12. (a) (i) Design a network with four inputs and three outputs which realizes the following functions.

$F_1(a, b, c, d) = \Sigma m(11, 12, 13, 14, 15)$

$F_2(a, b, c, d) = \Sigma m(3, 7, 11, 12, 13, 15)$

$F_3(a, b, c, d) = \Sigma m(3, 7, 12, 13, 14, 15)$. (8)

(ii) Explain the operation of the tristate TTL inverter. (8)

Or

(b) (i) Design a combinational logic circuit that will generate the square of all the combinations of a 3 bit binary number. (8)

(ii) Find the reduced POS form of the following equation $F(a, b, c, d) = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5)$. Implement using NAND logic. (8)

13. (a) (i) Implement the following Boolean function using 8 : 1 MUX. (8)

$$f(a, b, c, d) = a'bd' + acd + b'cd + a'c'd$$

(ii) Implement the following functions using PLA :

$F_1(x, y, z) = \Sigma m(1, 2, 4, 6)$

$F_2(x, y, z) = \Sigma m(0, 1, 6, 7)$

$F_3(x, y, z) = \Sigma m(2, 6)$. (8)

Or

(b) Design a BCD code to 7 segment display Decoder network. (16)

14. (a) Design a MOD–5 synchronous counter using JK flip–flop. (16)

Or

(b) Design a sequence detector circuit to generate a high output when the input sequence is 101. Overlapping sequences are allowed. (16)

15. (a) (i) Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows :

$$Y = x_1x_2 + x_1y_2 + x_2y_1$$

$$Y = x_2 + x_1y_1y_2 + x_1y_1$$

$$Z = x_2 + y_1 .$$ (8)

(ii) Derive the SM chart for binary divider and binary multiplier. (8)

Or

(b) (i) Give the hazard free realization for the following functions. (8)

$$f(a, b, c, d) = \Sigma m(0, 2, 6, 7, 8, 10, 12)$$

(ii) Explain how can essential hazards be determined from the flow table and how it can be eliminated from the network. (8)
