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K 6446

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Elective

VLSI Design

VL 1622 — LOW POWER VLSI DESIGN

(Common to ME – Applied Electronics)

(Regulation 2005)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

What is the need for low power in VLSI design?

State the effect of LDD structure in CMOS design.

List the key principles involved in low power design.

What is Gate Delay Model?

5. State the various issues involved in the reduction of power consumption in memories.
6. What is meant by memory bank?
7. Give reasons why clock masking is obsolete today.
8. What are the factors that affect circuit reliability?
9. Justify the statement : To reduce dynamic power the gates that toggle at higher frequency should be made smaller.
10. What are levels at which the improvements in power dissipation are possible?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Enumerate on the figure of merits that is used for measuring power efficiency in a chip or a system.
(ii) Discuss the various effects that influence the threshold voltage of MOSFET.

Or

- (b) (i) Draw and explain the circuit of a CMOS Inverter and obtain the expression for short-circuit power dissipation of unloaded inverter.
(ii) Briefly summarize the hierarchy of theoretical limits.
12. (a) (i) With an example, explain the optimization procedure using operation reduction. What are its adverse effects?
(ii) Differentiate between area optimization and power optimization.

Or

- (b) Discuss the different methods for reducing power consumption in CMOS logic circuits.
13. (a) (i) Explain how Banked organisation of SRAMS is an efficient way to reduce switched capacitance.
(ii) Briefly explain the techniques used to reduce voltage swings on lines.

Or

- (b) Differentiate between adiabatic logic computation and static CMOS logic. Explain with relevant circuits and waveforms.
14. (a) Explain the Gate-level logic simulation technique. What are its merits and demerits.

Or

- (b) Discuss the power estimation of CMOS combinational and sequential logic circuits using entropy.
15. (a) How does software optimization lead to low power? Explain.

Or

- (b) Explain the role of behavioural level transforms in reducing power dissipation. Briefly discuss the techniques involved.