Reg. No. : | | | | | | | | | | | |

K 6454

M.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Second Semester

VLSI Design

VL 1651 — COMPUTER AIDED DESIGN OF VLSI CIRCUITS

(Common to M.E. — Applied Electronics)

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Distinguish between tractable and intractable problems.

2. List out the entities to be optimized during VLSI design.

3. What are the important issues to be considered for compaction?

4. How can placement algorithms be grouped and give example for each?

5. What are the different approaches to solve global routing problems?

6. List the factors considered for floor planning.

7. What are the most important delay modeling?

8. Compare compiler driven simulation and event driven simulation.

9. What are the goals of High level synthesis?

10. Give an example for conditional data flow graph.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Describe the different design methodologies and compare them. (8)

(ii) Describe the steps of VLSI design cycle and explain all the stages of physical design cycle. (8)

Or

(b) (i) Formulate on efficient algorithm for searching graphs and explain with examples. (10)

(ii) What are the different VLSI design automation tools and explain briefly about them? (6)

12. (a) (i) Discuss the Kernighan-Lin partitioning algorithm with suitable example. (10)

(ii) Compare the efficiency of simulated annealing and simulated evolution algorithms and in what respects do these algorithms differ. (6)

Or

(b) (i) Formulate an efficient algorithm for constraint graph compaction with examples. (12)

(ii) List the most common types of minimum distance rules and discuss briefly. (4)

13. (a) (i) Describe the shape functions and floor plan sizing. (8)

(ii) Discuss the various parameters which define different rooting problems. (8)

Or

(b) What are the different approaches to solve global rooting problem? Write an efficient algorithm to find a path between a pair of points in a rectangular grid. (16)

14. (a) (i) Explain in detail the specific simulation tools for different abstraction levels. (8)

(ii) Explain in detail the important issues related to gate level simulation. (8)

Or

(b) (i) Describe briefly the switch level modeling and simulation. (8)

(ii) Explain in detail two level logic synthesis with example. (8)

15. (a) Explain various scheduling algorithms in High level synthesis and compare them. (16)

Or

(b) (i) Explain DFG and issues related to optimization of High level synthesis. (10)

(ii) Discuss the goals and terminology of allocation. Assignment and scheduling. (6)
