G 7052

M.E. DEGREE EXAMINATION, JANUARY 2006.

First Semester

Computer Science And Engineering

CS 1601 — COMPUTER ARCHITECTURE

(Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define Spatial locality and Temporal locality.

2. List out the types of architecture and its advantages and disadvantages.

3. What do you mean by Address value prediction and speculation?

4. What are the functions of Branch history table?

5. What are the effects of unrolling?

6. Define loop – carried dependence with an example.

7. Define Dirty bit and misspenalty.

8. What is critical word first and early restart?

9. Define Snooping.

10. List out the advantages of message passing communications.

PART B — (5 × 16 = 80 marks)

11. (i) With necessary example explain the different types of addressing modes. (8)

(ii) Explain the different classification of instruction set architecture. (8)

12. (a) What are different types of dependencies and explain each w necessary example?

Or

(b) Explain Dynamic scheduling using Tomasulo's approach with necessary diagram.

13. (a) Discuss Intel IA-64 architecture and itanium processor.

Or

(b) (i) Narrate the crosscutting issues between Hardware versus softwar speculation mechanism.

(ii) Consider the following loop. Find out what are the dependence between S_1 and S_2? Is this loop parallel? If not show how to mak it parallel?

```
for (i = 1; i < = 100; i = i + 1) {
A[i] = A[i] + B[i]; / * S1 * /
B[i + 1] = C[i] + D[i]; / * S2 * /
}
```

14. (a) Write a detail note on :

(i) block placement (4)

(ii) block identification (4)

(iii) block replacement (4)

(iv) write strategy. (4)

Or

(b) Explain different levels of RAID with an example. (16)

15. (a) (i) What is Cache coherence problem in multiprocessor? Explain with necessary example. (8)

(ii) Explain the Basics of Directory – Based cache coherence protocols in distributed shared memory architecture. (8)

Or

(b) Explain in detail about synchronization in multiprocessors and thread level parallelism. (16)
