E 8222

M.C.A. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2005.

First Semester

CA 134 — COMPUTER ARCHITECTURE

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw a two-input to four-output decoder.

2. What is clocked D flip-flop?

3. What is the use of the following instructions?

   (a) BSA

   (b) CIL

4. Write a routine to pack two BCD digits into a byte.

5. Define cache and virtual memory.

6. What is the need for memory management?

7. Define DMA.

8. Give the application and uses of SCSI bus.

9. State the important speedup features of modern computers.

10. Give an example of pipelining.

PART B — (5 × 16 = 80 marks)

11. (i) Explain in detail the address translation with segmentation and paging. (8)

    (ii) Describe about associative memory. (8)

12. (a) (i) Give the implementation of the up/down counter using requential circuit with state diagram of a mod-4 up/down counter that detects the count of 2. (12)

(ii) A truth table has a low output for the first three input conditions : 000, 001 and 010. If all the outputs are high, what is the product of sums circuit. (4)

Or

(b) (i) Design a finite state machine for modulo-4 counter. (8)

(ii) Implement the PLA realization of a full adder. (8)

13. (a) (i) Design a control unit for the 2's complement multiplier. 8)

(ii) Explain the block diagram of microcoded control unit. (8)

Or

(b) (i) Design a 4 bit ALU with carry look-ahead signals. (8)

(ii) Explain the various addressing modes with suitable examples. (8)

14. (a) (i) Discuss how program controlled I/O is performed using polling. (8)

(ii) Write a brief description on CD-ROM storage device. (8)

Or

(b) (i) With block diagram explain the combined input/output interface circuit. (8)

(ii) Explain the idea of interrupts and the hardware/software needed to support them. (8)

15. (a) (i) Differentiate between RISC versus OISC Architecture. (8)

(ii) Explain the pipeline organization of the ultraSPARC II processor. (8)

Or

(b) Give a detailed description of the case study of any one parallel architecture. (16)
