N 1249

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2004.

Fourth Semester

Computer Science and Engineering

CS 238 — COMPUTER ARCHITECTURE – I

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compute the effective CPI for a processor, for the following instruction mix :

Instruction type	Clock cycle count	Frequency
ALU operations	1	40
Loads	3	20
Stores	2	10
Branches taken	3	20
Branches not taken	2	10

An enhancement to the processor is made by adding a branch prediction unit. This decreases the number of cycles taken to execute a branch from 3 to 2. What is the improvement in performance?

2. Give example for the following addressing modes with an example :

   (a) Register indirect addressing

   (b) Relative addressing.

3. State the IEEE standard for single precision floating point numbers and explain.

4. State the principle of operation of a carry–look–ahead adder.

5. State the different types of hazards that can occur in a pipeline.

6. What are the relative advantages and disadvantages of microprogrammed control over hardwired control?

7. What is meant by memory interleaving? Show the distribution of addresses for a memory system consisting of two banks of four 1K memory modules to form an 8K memory system. Give the main memory address format.

8. What is a TLB? What is its significance?

9. Distinguish between a synchronous bus and an asynchronous bus.

10. How does a processor handle an interrupt?

PART B — ($5 \times 16 = 80$ marks)

11. (i) Give the organisation of the internal datapath of a processor that supports a 4–stage pipeline for instructions and uses a 3–bus structure and discuss the same. (10)

(ii) What is meant by dynamic branch prediction? Discuss the operation of a 2–bit dynamic branch predictor. (6)

12. (a) (i) Discuss the different issues to be considered while designing the instruction set architecture (ISA) of a processor. (10)

(ii) Distinguish between RISC and CISC processors. (6)

Or

(b) (i) Show a possible control sequence for supporting sub–routine calls on a processor with a single bus organisation. Assume that a stack is used to save the return address. The subroutine call is initiated by a CALL ADDR instruction made up of two words with ADDR occupying one word and using direct addressing. The return instruction is a single word RET instruction. (10)

(ii) Give the control sequence for executing the single word instruction.

ADD (R_0), R_1, (R_2) where the first two are the source operands and the third is the destination operand for a single bus organisation. (6)

13. (a) (i) Give the schematic of a 4×4 array multiplier and explain. What is the worst case delay in this case? (8)

(ii) Give the organisation of a sequential binary multiplier and explain. (8)

Or

(b) (i) State the non–restoring division technique. Simulate the same for $20 \div 8$. (10)

(ii) What is a carry–save adder? Discuss with an example. (6)

14. (a) (i) Discuss the relative advantages and disadvantages of the three mapping techniques used in Cache memories. (10)

(ii) Consider a main memory of size 128 MB and a Cache of size 64 kB. If the block size is 64 bytes and the Cache uses 4–way set–associative mapping, give the main memory address format and explain. (6)

Or

(b) (i) Discuss any one virtual memory management technique in detail. (10)

(ii) What are associative memories? How are they constructed? How are they useful? (6)

15. (a) (i) What is a DMA transfer? Explain in detail how this is accomplished. (10)

(ii) Distinguish between memory–mapped I/O and I/O mapped I/O. (6)

Or

(b) Discuss the design of a typical input or output interface. (16)
