N 1152

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2004.

Fourth Semester

Electronics and Communication Engineering

EC 242 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Perform 2s complement subtraction of 010110 – 100101.

2. What is the advantage of biquinary code?

3. What are universal gates?

4. Obtain 3–level NOR–NOR implementation of $f(a, b, c) = [ab + cd]ef$.

5. Define fan in.

6. Draw the circuit diagram of a HTL NAND gate.

7. Derive T FF from JK FF.

8. Draw the timing diagram of 4 bit ring counter.

9. What is an asynchronous sequential circuit?

10. When do hazards occur?

PART B — ($5 \times 16 = 80$ marks)

11. Obtain the primitive flow table for an asynchronous circuit that has two inputs x, y and one output z. An output $z = 1$ is to occur only during the input state $xy = 01$ and then if and only if the input state $xy = 01$ is preceded by the input sequence $xy = 01, 00, 10, 00, 10, 00$.

12. (a) Use Tabulation method to simplify

$F\ (A, B, C, D, E, F, G) = \Sigma(20, 28, 38, 39, 52, 60, 102, 103, 127)$.

Or

(b) Design a BCD to Gray code converter. Use don't cares.

13. (a) Explain with a circuit the working of three–state TTL gate.

Or

(b) Explain the operation of 2–input CMOS NAND and NOR gates.

14. (a) Design a seven segment decoder circuit to display the numbers 0 to 3.

Or

(b) Explain carry look ahead adder circuit.

15. (a) Explain the parallel load – serial out data transfer operation in a 4 bit shift register.

Or

(b) Explain the working of BCD ripple counter with timing diagrams.
