K 1310

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2004.

Fifth Semester

Electrical and Electronics Engineering.

EE 334 — INTEGRATED CIRCUITS

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. How surface layer of SiO_2 is formed?

2. Explain what is meant by parasitic capacitance in an IC.

3. Draw a circuit using operational amplifier to convert square wave to triangular wave.

4. Calculate the output voltage V_0 of the circuit shown in Fig. Q. 4

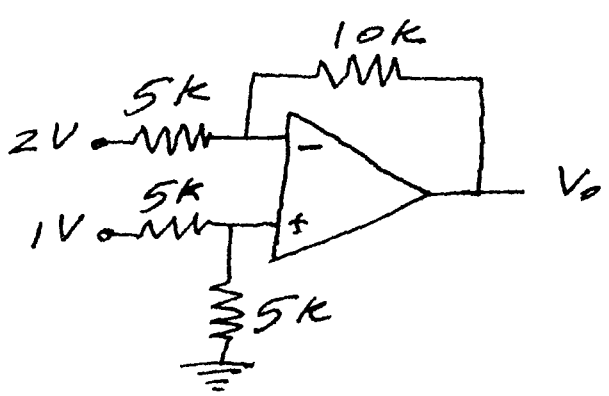

Fig. Q. 4

5. Realize the function $Y = A + B + C$ using NAND gates.

6. Draw the circuit of a half subtractor.

7. Draw the circuit of CMOS inverter used in VLSI circuits.

8. What is meant by catch–up in CMOS IC technology?

9. An A/D converter has a conversion time of 1 micro seconds. Calculate the maximum frequency at which it can be used.

10. An 8 bit D/A converter has output voltage range of 0–5 volt. Calculate the change in its output voltage when the least significant bit of the input changes.

PART B — ($5 \times 16 = 80$ marks)

11. Draw the circuit of a CMOS inverter and explain the steps involved in its fabrication using n–well or p–well process.

12. (a) (i) Draw the circuit of a first order active low pass filter and derive an expression for its transfer function.

(ii) Derive an expression in the form of a differential equation for the output voltage $v_0(t)$ of the circuit shown in Fig. Q. 12 (a)(ii).

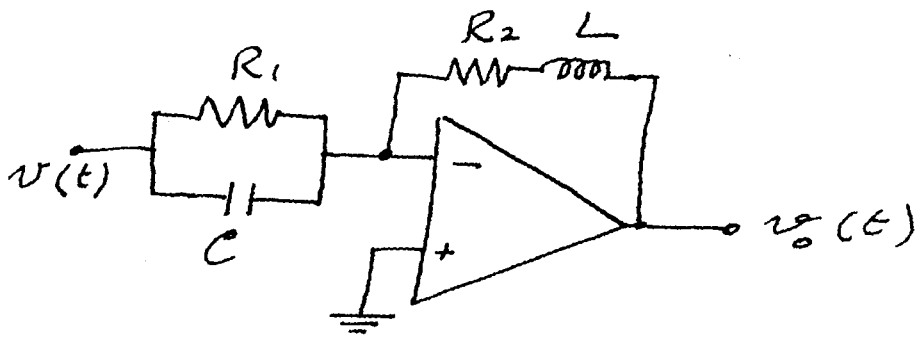

Fig. Q 12 (a) (ii)

Or

(b) (i) Draw the circuit of a phase shift oscillator using operational amplifier and derive an expression for the condition of oscillation and frequency of oscillation.

(ii) Design a monostable multivibrator for a time delay of 1 second using the IC NE 555. Derive any formula used.

13. (a) (i) Draw the circuit of a CMOS NAND gate.

(ii) Design a synchronous decade counter using J–K flip–flop.

Or

(b) (i) Draw the circuit of a dynamic RAM cell and explain its worki ıg.

(ii) Show the realization of 1 kilo byte RAM using 256×4 bit RAM ICs.

14. (a) Draw the circuit of a NMOS inverter and derive an expression for its pull up to pull down ratio.

Or

(b) With neat diagram explain the structure and working of an enhancement mode and depletion mode types of MOSFETS used in VLSI circuits.

15. (a) (i) With neat diagram explain the working of dual slope type ADC.

(ii) In a dual slope type ADC the reference voltage of 2 volt is to be integrated for 20 milli seconds. The magnitude of peak output of the integrator is 5 volt. The value of the integrator capacitor is 0.1 μF . Calculate the value of the integrating resistor.

Or

(b) Describe the principle of switched capacitance filter. Explain how it can be realized using special ICs.
