N 1255

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2004.

Sixth Semester

Computer Science and Engineering

CS 340 — COMPUTER ARCHITECTURE – II

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the Amdahl's Law.

2. List out the distinct features between RISC and CISC architectures.

3. What are Data Hazards in Pipelining?

4. What is Dynamic Scheduling?

5. What are Multiple Issue Processors? Give an example.

6. Why it is important to find the dependences in a program?

7. What are the main components of distributed memory architecture?

8. State the principle of write Invalidate Protocol.

9. List the important characteristics of I/O buses.

10. What are the two main addressing modes supported by SPARC RISC architecture?

PART B — (5 × 16 = 80 marks)

11. (i) Explain in detail the architecture of a RISC processor. (8)

(ii) Discuss about Data Flow Systems. (8)

12. (a) (i) Describe the Quantitative Principles of Computer Design. (8)

(ii) Discuss about the different types of Instruction Set Architectures. (8)

Or

(b) (i) Enumerate the important parameters involved in the performance evaluation of computer architectures. (8)

(ii) Discuss about the computer related issues in designing the computer architectures. (8)

13. (a) (i) Explain the Instruction Execution using Pipelining Process. Bring out the performance issues in Pipelining. (8)

(ii) Discuss about Structural Hazards in Pipelines. (8)

Or

(b) (i) Explain in detail the different types of dependences in programs. (8)

(ii) Explain the dynamic Branch Prediction Scheme. (8)

14. (a) (i) Explain in detail the Super Scalar approach for implementing a multiple issue processor. (8)

(ii) Explain the architecture of VLIN processor. State the limitations of this processor. (8)

Or

(b) (i) Explain the architecture and function of a Vector Processor. (8)

(ii) Discuss about the compiler support for ILP. (8)

15. (a) (i) Explain the performance metrics for communication mechanisms used in multiprocessors. (6)

(ii) Compare centralized and distributed memory architectures. (10)

Or

(b) Explain what is Multiprocessor Cache coherence. Discuss in detail the protocols to maintain coherence for multiple processors. (16)
