K 1221

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2004.

Third Semester

Information Technology

IF 242 — DIGITAL SYSTEM DESIGN

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Find the octal equivalent of decimal 200.

2. Determine the product of all 2^n maxterms of n variables.

3. Why is gold doping often used in switching transistors?

4. When compared with TTL, what are the disadvantages of ECL?

5. Write down the truth table of a half subtractor.

6. What is a (p, n, m) PLA?

7. What is a PROM?

8. How will you convert a JK flip–flop into a D flip–flop?

9. With reference to the state diagram of a sequential machine, what are source states and sink states?

10. State Unger's theorem.

PART B — ($5 \times 16 = 80$ marks)

11. (i) Express $x + yz$ as the product of maxterms. (6)

(ii) Minimise the switching function

$$F(x_1\ x_2\ x_3\ x_4) = \Sigma(1, 4, 5, 7, 13) + \Sigma_\phi(0, 6, 14, 15)$$

on a 4 variable Karnaugh map. (10)

12. (a) (i) Draw and explain the circuit diagram of a DTL NAND gate. (12)

(ii) With reference to TTL, what is the current spike problem? (4)

Or

(b) (i) Explain how an EX–OR gate can be built by using four NAND gates. (4)

(ii) The output of a NAND gate network is $F(ABC) = \Sigma(3, 6, 7, x)$. The output of the gate network does not change if all the gates are replaced by NOR gates. Determine the value of x. (12)

13. (a) (i) Show that when two 2 i/p multiplexers drive another 2 i/p MUX, the result is a 4 i/p multiplexer. (6)

(ii) Derive the PLA implementation of a serial binary adder. (10)

Or

(b) (i) Show that when a 3 line to 8 line DEMUX drives eight 3 line to 8 line DEMUXs, the result is a 6 line to 64 line DEMUX. (10)

(ii) How will you build a 4 bit comparator using a single 7485? (6)

14. (a) (i) What is the characteristic equation of a D flip–flop? (4)

(ii) Using JK flip–flops, design a parallel counter which counts in the sequence 101, 110, 001, 010, 000, 111, 101, ... (12)

Or

(b) (i) Explain the significance of the following statement :

'There can be a number of sequential circuits implementing the same sequential machine'. (4)

(ii) A synchronous sequential machine produces an output of 1 when exactly two 1's are followed by one 0. Once the output becomes a 1, it remains so until the sequence 10 is received, when the output returns to 0. Derive the minimised state table for the machine. (12)

15. (a) (i) Implement the switching function $f(x_1\ x_2\ x_3) = x_1\bar{x}_2 + x_2\,x_3$ by a static hazard free 2 level AND–OR gate network. (8)

(ii) Show that dynamic hazards do not occur in 2 level AND–OR gate networks. (8)

Or

(b) Write short notes on :

(i) asynchronous sequential circuits. (8)

(ii) VHDL. (8)
